TSC01/11 TAPE STREAMER COUPLER

TECHNICAL MANUAL

ISKRA DELTA COMPUTERS

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CHAPTER 1

INTRODUCTION

1.1 SCOPE

This manual provides information related to the capabilities, design, installation, and use of the IDC TSC01/11 Tape Streamer Coupler. The manual also provides applicable diagnostic and application information.

The contents of the five sections and appenidc in this manual are brifly outlined in the following descriptions:

Section 1	Introduction: This section contains an overview of the TSC01/11 and includes the specification.
Section 2	General Description: This section includes the description of a physical characteristics and interfaces.
Section 3	Coupler Registers and Programming: This section describes the registers and the command packets.
Section 4	Installation: This section conatins the information necessary to set-up and physically install the Tape Coupler system.
Section 5	Troubleshooting: This section describes fault isolation procedures that can be used to pinpoint trouble spots.
Appendix A	TSC01/11 Tape Coupler Option Switches: This

appendix provides instructions for configuring the TSC01/11 Tape Coupler and for selecting options by means of switches.

1.2 OVERVIEW

The TSC01/11 Magnetic Tape Coupler emulates the TS11 tape coupler manufactured by the Digital Equipment Corporation (DEC). The TSC01/11 tape coupler functions with both streaming and start/stop tape transports.

The TSC01/11 tape coupler is hardware compatible with Pertec or equivalent start/stop formatted tape transport systems that ooerate with the nine-track Non-Return to Zero Inverted (NRZI) format at the 800 characters per inch (cpi), or in Phase Encoded (PE) format at 1600 cpi, or in Group Code Recording (GCR) format at 6250 cpi.

System tape transports may ooerate at any of the industry standard tape speeds from 12.5 to 125 inches per second (ips).

1.3 FEATURES

The TSC01/11 tape coupler design incorporates several features that enhance usfulness, serviceability, and performance.

1.3.1 MICROPROCESSOR ARCHITECTURE

The main part of the controller is a bit slice designed Microprocessor using two AM 2901C ICs.

The Microprocessor gets data to D-inputs from the Pipeline register or from the D-bus, which is the controller PCB major data path (see FIg. 2-1). Microprocessors' data outputs are the only data sources for Y-bus. Y-bus destination are various address pointers. Data can be transferred from Y-bus to the D-bus.

The sequencer for the Microprocessor consists of one AM 2910 IC. The 2910 Sequencer provides the capability for addressing the control store from its program counter, 'SI-bits' literal field, internal P-register or internal ten-level Stack-file. The

Sequencer performs jumps, conditional jumps, subroutine jumps and subroutine returns. Up to 32 individual jump conditions can be tested. As a special feature the Sequencer tests the Microprocessors' ALU status flags (CARRy, MINUS, ZERO) only for the current executing micro-instruction. The next address generation is based on the results of the arithmetic operation and microprogram memory is accessed accordingly.

Microprogram execution could be interrupted if Tape or Unibus microinterrupts occurred. Each of the interrupts can be masked for a period of time when the Microprocessor is performing a time-critical function. Tape interrupts occur during tape read or write operations whenever the Read or Write buffer-register is full or empty. The Interrupt Control Logic provides an interrupt vector determined by the operation requested from the Unibus or tape drive. During the interrupt execution the 2910 outputs are disabled (CARRY IN in the Sequencer is held "0"). The Interrupt control Logic performs jump to Interrupt-Starting-Microinstruction, containing a 2910-s "JSR" instruction. The Interrupt-Ending-Microinstruction (containing a "RTS" instruction) continues the "normal" microprogram-flow. There is only one "nonmaskable" interrupt input, handling the Power-up init, Unibus init and the WDT (Watch Dog Timer). If such an interrupt occurs, the microprogram sequencer starts an execution of the microprogram from the address zero.

1.3.2 SELF TEST

The TSC01/11 tape coupler firmware incorporates an internal Self-Test routine which is executed when the computer/tape transport system is powered up. This test exercies all parrs of the microprocessor, buffer, and data handling logic. This self test does not completly test all circuitry in the TSC01/11 coupler, but successful completion indicates hig probability that all circuts in the TSC01/11 tape coupler are operational.

1.3.3 BUFFERING

The TSC01/11 tape coupler includes 3840 bytes of data buffering and it transfers data to or from memomry on a word basis, except for odd bytes at the start or end of the record.

1.3.4 SPECIFICATION

Specifications for the TSC01/11 tape coupler are listed and described in Table 1-1.

Table 1-1. TSC01/11 Specifications

Parameter	Characteristic
FUNCTIONAL	
Number of Tape Transport Emulations Supported	Up to 4
Tape Speeds	All standard tape speeds rom 12.5 to 125 ips
Tape Transport Interface	Pertec
Media Compatibility	1/2-inch wide magnetic tape per ANSI Standard X3.40-1976
Data Block Capacity	Up to 65,535 data bytes
Priority Level	BR5
Data Buffering	3840 bytes
Data Transfer	DMA via Unibus, 16-bit word, except for odd byte at beginning or enf of record
Self-Test	Extensive internal self-test on powering up
Indicators	Three LEDs for activity status indications
DESIGN	High-speed, bipolar microprocessor with AMD 2901-type bit-slice components
PHYSICAL	
Mounting	Any SPC slot in standard DEC PDP-11 or VAX-11 central processing unit (CPU)
Cables	Two 50-wireflat cables

Table 1-1. TSC01/11 Specifications

Parameter	Characteristic
ELECTRICAL	
Power	+5 Volts (V), 4.5 Amperes (A)
Unibus Interface	DEC approved line drivers and line receivers
Tape Transport Interface	Open collector line drivers and TTL receivers. Cable length accumulative to 30 feet.
ENVIRONMENTAL	
Operating Temperature	0 to 55 Celsius (C)
Storage Temperature	-10 to 70 Celsius
Relative Humidity	10 to 90 percent, noncondensing

CHAPTER 2

GENERAL INFORMATION

2.1 PHYSICAL DESCRIPTION

The TSC01/11 Streamer Tape Coupler is constructed on a single quad-size printed circuit board. This board contains all circuitry required to control streaming tape transports.

2.1.1 Connectors

The coupler is interfaced to the tape transport via two 50-pin connectors J1 and J2.

An additional male connector is designed (J3),which is used for connecting a special test device, purposed for factory tests and repair operations, and is not intended for use in normal coupler operations.

2.1.2 Switches and jumpers

The 8-pole DIP, 4-pole PIANO switches and jumpers W7-W12 are used for coupler options.

2.1.3 Indicators

The three LEDs (CR1, CR2, CR3), located on the board, indicate tape activity without data transfer, data transfer activity and coupler ready status.

After succesful power-up self-test sequence the LED CR3 should be lit and TSC01 is ready.

If the self test fails, the three LEDs will be lit, displaying the error condition.

2.1.4 Connectors and Cables

The tape coupler uses two 50-conductor flat cables to interface to the transports. The cable should be a twisted pair with a maximum daisy-chained length of not over 30 feet. All wires should be 24 AWG minimum, and each pair should not have less than one twist per inch. Connectors are standard 50-pin flat cable connectors.

2.1.5 Signal Definitions

Signal definitions are grouped by direction of a signal flow; from the tape coupler to the embedded formatter on the tape transport, or the tape coupler from the embedded formatter on the tape transport.

2.1.5.1 Coupler to Formatter -

Transport Address: TAD0,TAD1

These lines determine which of up to four transports is selected by the coupler. TAD1 is the most significant bit.

Formatter Address: FAD

This signal selects one of two formatters. It is always zero for this emulation.

Initiate Command: GO

A pulse which initiates any command specified by a combination of the command signals REVERSE, WRT, WFM, ERASE, EDIT, LGAP and/or HSPD.

Rewind Command: REWIND

A low level pulse of approximately one microsecond commands the selected transport to rewind to the load point.

Unload Command: UNL

A low level pulse of approximately one microsecond causes the selected tape transport to go off-line, to rewind the tape, and when BOT is encountered, to unload the tape onto the supply reel.

NOTE: Some tape drives do not support this feature and will go off-line

without rewinding.

Write: WRT

Write mode is specified when this signal is TRUE; read mode is specified when it is FALSE.

Write File Mark: WFM

When this signal and WRT are TRUE, the transport will write a file mark on the tape.

Erase: ERASE

When ERASE and WRT are TRUE, the transport executes a dummy write command. The transport will go through all the operations of a normal write command but no data will be recorded. A length of tape will be erased equivelent to the length of the Dummy record (as defined by LWD). If ERASE, WRT and WFM are TRUE, the transport will execute a dummy write file mark command. A fixed length of tape of approximately 3.75 inches will be erased.

High Speed: HSPD

If this signal is TRUE when a read or write command is issued, the transport will read or write at the high speed.

Last Word: LWD

When TRUE during a write or erase command, this signal indicates that the next character to be strobed into the transport (formatter) is the last character of the record.

Reverse: REVERSE

When TRUE, this signal initiates reverse tape motion. When it is FALSE, forward tape motion is specified.

Edit: EDIT

This is a signal which, when TRUE during a read reverse operation, modifies the read reverse stop delay to optimize head positioning for a subsequent edit operation. When EDIT and WRT are TRUE, the selected transport operates in the edit mode.

Formatter Enable: FEN

When FALSE this signal causes the transport to be held in an initialized state.

Write Data 7:0, Parity: WD7:WD0, WDP

These lines transmit data to the transport. Line zero is the most significant. WDP carries the odd parity bit associated with each data word. The parity bit is generated by the coupler.

Long Gap: LGAP

When TRUE, this signal causes the transport to generate 1.2 in. long IRG. Not supported at the moment of printing.

Density: DEN

When used with a dual-mode transport, the TRUE level selects NRZI and the FALSE level selects P.E. Not supported at the moment of printing.

2.1.5.2 Formatter to Coupler -

Formatter Busy: FBY

When TRUE, this signal inhibits further commands to the formatter. The signal becomes TRUE on the trailing edge of GO when a command is issued by the coupler. FBY remains TRUE until a new command is given.

On-Line: ONL

A low level indicates that the selected tape transport is on-line and under control of the tape coupler.

Ready: READY

A low level indicates that the selected tape transport is loaded and not rewinding.

Rewinding: RWD

A low level indicates that the selected tape transport is engaged in a rewind operation or, the load sequence is following a rewind operation.

End of Tape: EOT

A low level indicates that the EOT tab on the tape is being sensed.

Beginning of Tape: BOT

A low level indicates that the selected tape transport is sensing the BOT tab on the tape, has completed its initial load sequence, and the tape transport is not rewinding.

File Protect: FPT

A low level indicates that a reel tape, mounted to the transport, does not have a write enable ring installed.

Data Busy: DBY

This signal becomes TRUE after a command has been accepted by the transport. DBY remains TRUE until the data transfer is completed

and the appropriate post record delay has expired.

Hard Error: HER

A TRUE pulse of this signal indicates that an uncorrectable read error has occured and that the record should either be reread or rewritten.

Corrected Error: CER

A TRUE pulse of this signal indicates that a single track dropout has been detected and the formatter is performing an error correction.

Identification: PEID

When TRUE, this signal indicates that a PE identification burst has been detected. When in 800 bpi mode (NRZI), this signal is TRUE when the read information being transmitted to the coupler is a cyclic redundancy check character (CRCC) or a longitudinal redundancy check character (LRCC). It is FALSE when data characters are being transmitted.

File Mark: FMK

This signal is pulsed when a file mark is detected on the tape during a read operation or during a write file mark operation in a read-after-write transport.

High Speed Status: HSPS

When TRUE , this signal indicates that the selected transport is in the 100 ips (streaming) mode. A FALSE level indicates that the transport is operating at low speed (start/stop).

NRZI Mode: INRZ

This signal is TRUE when the transport is in 800 bpi mode (NRZI). Not supported at the time of printing.

Write Data Strobe: WDS

This signal is pulsed each time a data character is written onto tape. WDS samples the write data lines WDP, WD7:WD0 from the coupler and copies this information character by character into

the formatter write logic. The first character should be available prior to the first write strobe pulse and succeeding characters should be set up within half a character period after the trailing edge of each write strobe.

Read Data Strobe: RDS

This signal consists of a pulse for each character of read information to be transmitted to the coupler. Leading edge of this signal is used to sample the read data lines RDP, RD7:RD0.

Read Data 7:0, Parity: RD7:RD0, RDP

Each character read from tape is made available by parallel sampling the read lines to RDS. Since the data remains on the read data lines for a full character period, corresponding RDS pulses are timed to occur after approximately the center of the character period.

2.2 UNIBUS INTERFACE

The coupler interfaces to the PDP-11 or VAX-11 Unibus via a Small Peripheral Controller (SPC) connector. The Unibus consists of 18 address lines and 16 bi-directional data lines, plus control signals for data and interrupt vector address transfer and for becomming bus master.

2.2.1 BR (Interrupt) Priority Level

The coupler is hardwired for BR5. The other three Bus Grant signals are jumpered through.

2.2.2 Register Addresses

The addresses which are assigned to the coupler's registers are selected from a range of four address groups. Each group contains contiguous starting addresses for four TS11 emulations. The emulations require only two Unibus register addresses a piece.

2.2.3 Interrupt Vector Address

The interrupt vector addresses for the four TS11 emulations provided by the TSC01/11 are switch selectable.

2.2.4 DCLO and INIT Signals

The DCLO and INIT signals both perform a coupler clear.

2.2.5 NPR Operations

All DMA data transfers are carried out under microprocessor control. A check is made for memory parity errors when doing a tape write operation. If an error is detected, the Unibus Parity Error (UPE) error is set.

CHAPTER 3

COUPLER REGISTERS AND PROGRAMMING

3.1 OWERVIEW

This section describes and defines the TSC01/11 registers and packet processing. In addition, programming examples and packet formats are provided to illustrate basic TSC01/11 programming concepts.

3.2 COUPLER REGISTERS

The DEC TS11 supports only a single tape transport. Therefore, each tape transport supported by the system has a unique set of Unibus registers and command/message buffers in CPU memory. The TSC01/11 supports four tape transports. Thus, the TSC01/11 is really emulating four TS11s with their attendant registers. It is, therefore, inaccurate to refer to TSC01/11 when discussing registers because the four register sets that the TSC01/11 contains are not related. For example, initializing one of the subsystem emulations by writing to the appropriate TSSR register does not affect the other three emulations. Also, it is not necessary (nor possible) to separate coupler command or status from transport command or status because each register and command/message buffer set is dedicated to the individual transport. Consequently, when discussing an individual emulation we will use the term transport instead of using emulation, TSC01/11 or TS11.

TSC01/11 TAPE COUPLER
COUPLER REGISTERS

Device register usage is compatible with DEC TS11 register definitions. However, some additions have been made to provide extended functions.

The eight transport registers are:

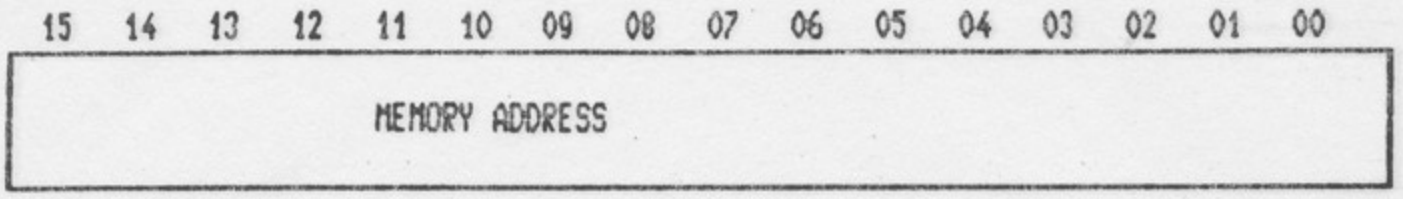
TSBA	(1)	- Unibus Address Register
TSDB	(1)	- Unibus Data Buffer
TSSR	(1)	- Status Register
XST	(5)	- Extended Status Registers

Each transport has two Unibus word locations used as device registers. The base address, when written to, is the data buffer register (TSDB). When read, it is the bus address register (TSBA). The second device register (base address + 2) is the status register (TSSR). Writing to the TSSR causes a subsystem initialize command , and reading the TSSR reads device status.

The TSDB register is the only register written during normal operations. DATO or word access must be used to properly write command pointers to the TSDB. DATOB or byte access to the TSDB causes maintenance functions.

Commands are not written to the transport's Unibus registers. Instead, command pointers, which point to a command packet somewhere in CPU memory space, are written to the TSDB register. The command pointer is used by the transport to retrieve the words in the command packet. The words of the command packet tell the transport the function to be performed. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

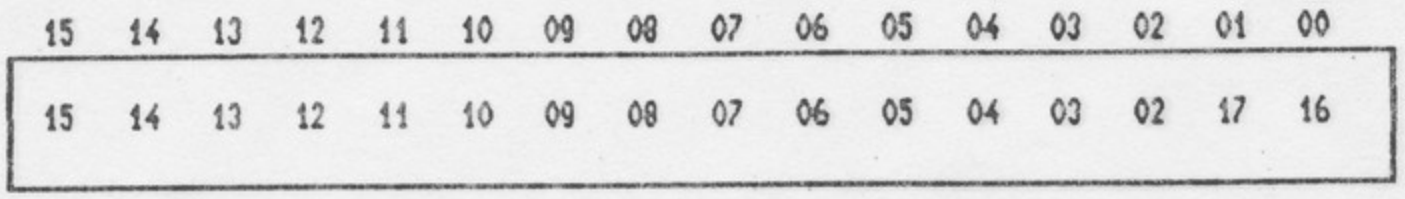
3.2.1 Base Address Register (TSBA)



The TSBA is a 16-bit register that is read at the transport's base address (17XXXX). It is a reflection of the least significant 16 bits of the 18-bit TSDB register. (TSDB bits 17 and 16 are displayed in TSSR bits 09 and 08, respectively.) The contents of TSBA are valid only after the termination of a command. (A command is initiated by loading a command packet address into TSDB.) The termination may be either with or without errors. The TSBA is the base address in the read only mode and it is not cleared at power up, subsystem INIT, or bus INIT. It can also be read at any time with or without the transport unit connected.

Upon completion of a command, the TSC01/11 deposits a message packet in a message buffer located in CPU memory. The TSBA may be read to determine the highest message buffer address plus two.

3.2.2 Data Buffer Register (TSDB)



The TSDB is an 18-bit register that is parallel loaded from the Unibus at the base address. The TSDB can be loaded when the transport is bus slave by three different types of transfers from a bus master. Two transfers are for maintenance purposes (DATOB to high byte and DATOB to low byte). The third transfer is for normal (word) operation (DATO). This register is write-only and is not cleared at power up, subsystem initialize or bus initialize. The transport responds with SSYN anytime the TSDB is written to.

3.2.2.1 Normal Operation -

A command is issued to the transport by loading an 18-bit address into the TSDB using a DATO. The address is that of a command packet located somewhere in Unibus address space. The address is loaded into the TSDB using the following format. Bits <15:02> of the register are loaded with bits <15:02>, respectively, from the Unibus. Bits 16 and 17 of the address are loaded from bits 00 and 01, respectively, from the Unibus. Bit 00 and bit 01 of the address are automatically loaded with zeroes by the transport logic. Loading the TSDB register initiates a fetch by the transport of the command packet at the specified address. The command defined in the packet is then executed.

3.2.2.2 Data Wraparound Using DATOB (odd) -

When TSDB is loaded by a DATOB to TSDB high byte (odd address), the following happens. Bits <07:00> of the register are loaded with bits <15:08>, respectively, from the Unibus. Bits <15:08>, respectively, from the Unibus. Bits 16 and 17 of the register are loaded with bits 08 and 09 respectively, from the Unibus. The TSDB is then loaded into TSBA. This transfer will be executed anytime a DATOB to the TSDB high byte is done. IF SSR (see TSSR bit 07) is clear, an error (RMR TSSR bit 12) occurs, but the transfer is still executed and completed. The TSSR is not affected (except for SSR bit 07, which gents cleared). To use the tape transport again, the CPU must initialize the transport (that is, write the TSSR).

3.2.2.3 Data Wraparound Using DATOB (even) -

When TSDB is loaded by a DATOB to TSDB low byte (even address), the following happens. Bits <15:00> of the register are loaded with bits <15:00>, respectively, from the Unibus. (Most PDP-11 CPUs assert all zeroes for bits <15:08> except for a MOVB; this sign extends bit 07. See the respective processor handbook for a MOVB instruction.) Bits 16 and 17 cannot be determined. The TSDB is then loaded into the TSBA. To use the tape transport again, the CPU must initialize the transport (that is, write the TSSR).

3.2.3 Status Register (TSSR)

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
SC	SPE	UPE	RMR	NXM	NBA	A17	A16	SSR	OFL	SIP	0	TC2	TC1	TC0	X

See Table 1-1 for definition of Termination Class (TC) Codes.

The TSSR is a 16-bit read/write register at base address 17XXXX+2. It can be read at any time with or without the transport unit connected. It can only be updated by the transport logic; it cannot be modified from the Unibus except indirectly. (SPE, UPE, RMR, NXM, and SSR bits are cleared when the TSDB is written by the host CPU.)

Any write function to the TSSR is decoded as a subsystem initialize. This resets the transport and coupler no matter what state they are in and causes an automatic load sequence returning the tape to BOT if the transport is on-line.

TSSR register bits 14 through 11 and 7 are cleared only at system power up, transport power up, subsystem initialize, or at the beginning of any write command to the TSDB register. Bits 15 and 07 are under control of the transport. These may be set or cleared independently of any transport operation. Bits 10 and <06:00> are controlled by the transport and reflect the subsystem status as indicated.

The TSSR register utilizes several bits to increase its status reporting capabilities. TSSR bits <03:01> report seven termination class status codes.

On fatal errors (termination class bits equal seven), if the need buffer address is not set (NBA=0), then the message may be valid. If the need buffer address is set (NBA=1), then there was no message.

The RMR bit will not affect the error class codes because RMR may occur on a bug free system. However, RMR will set the special condition (SC). (You may have tried to perform the next command while the transport was outputting the ATTN MSG.) If RMR is seen in the TSSR, the CPU must have written the TSDB while the command was executing.

The TSSR may not reflect the current state of the hardware if ATTNs are not enabled and the message buffer is not released. (That is, the transport may be off-line while the TSSR shows on-line). To keep the TSSR up to date would violate message packet protocol.

TSSR is not cleared immediately after initialization. The microprocessor runs to complete an automatic load sequence. When tape is at BOT, TSSR updates.

Special Condition (SC) - Bit 15

When set, this bit indicates that the last command was not completed incident-free. Specifically, either an error was detected or an exception condition occurred. An exception condition coud be a tape mark on read commands, reverse condition at BOT, EOT while writing, etc.

Unibus Parity Error (UPE) -Bit 14

This bit is set by the transport when it detects a parity error in the memory data being transferred from the CPU memory. (Causes TC4 and TC5.)

Serial Bus Parity Error (SPE) -Bit 13

This bit is set by the transport when it detects a serial bus parity error on data received from the transport. (Causes TC7.)

Register Modification Refused (RMR) - Bit 12

This bit is set by the transport when a command pointer is loaded into the TSDB and subsystem ready (SSR) is not set. This bit may be set on a bug free system if ATTN interrupts are enabled.

Nonexistent Memory (NXM) -Bit 11

This bit is set by the transport when trying to transfer to or from a memory location which does not exist. It may occur when fetching the command packet, fetching or storing data, or storing the message packet. (Causes TC4 and TC5.)

Need Buffer Address (NBA) - Bit 10

When set, this indicates that the transport needs a mesage buffer address. This bit is cleared during the set characteristics command if the transport gets valid data; it is always set after subsystem initialization.

Bus Address Bits 17:16 (A17, A16) -Bits <09:08>

A17 and A16 (bits 09 and 08) display the values of bits 17 and 16 in the TSBA register.

Subsystem Ready (SSR) -Bit 07

When set, this bit indicates that the transport is not busy and is ready to accept a new command pointer.

Off-Line (OFL) -Bit 06

When set, this bit indicates that the transport is off-line and unavailable for any tape motion commands.

Silo Parity Error (SIP) -Bit 05

This bit is set when the coupler detects a parity error on read data from the tape transport. (Causes TC7.)

Termination Class: TC02, TC01, TC00 - Bits <03:01>

These bits act as an offset value when an error or exception condition occurs on a command. Each of the eight possible values of this field represents a particular class of errors or exceptions. The code provided in this field is defined in Table 1-1. The code is expected to be utilized as an offset into a dispatch table for handling the condition. These bits are valid only when special condition (SC) is set. Refer to special conditions and errors, paragraph 3.3.3 of this manual.

Table 1-1
Termination Class Codes

TSSR Bits <03:01>	TC Code	Description
000	0	Normal termination
001	1	Attention condition
010	2	Tape status alert
011	3	Function reject
100	4	Recoverable error(tape position = one record down from start of function)
101	5	Recoverable error (tape not moved)

110	6	Unrecoverable error (tape position lost)
111	7	Fatal (Transport Data Parity) error

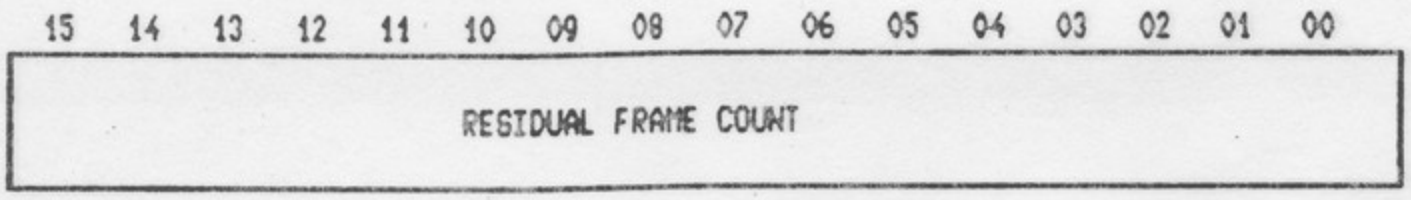
-

3.2.4 Extended Status Registers

Five additional registers are employed to provide additional status information: Residual Frame Count Register (RBPCR) and Extended Status Registers 0, 1, 2, and 3.

The extended Status Registers are not read directly from the registers accessible at the Unibus interface. At the end of a command or, by issuing a Get Status Command, the message packet information is updated. The end message packet, which results from the get status, contains the extended status words. This means that a message buffer has to be defined to the subsystem before the extended status registers are available to the software.

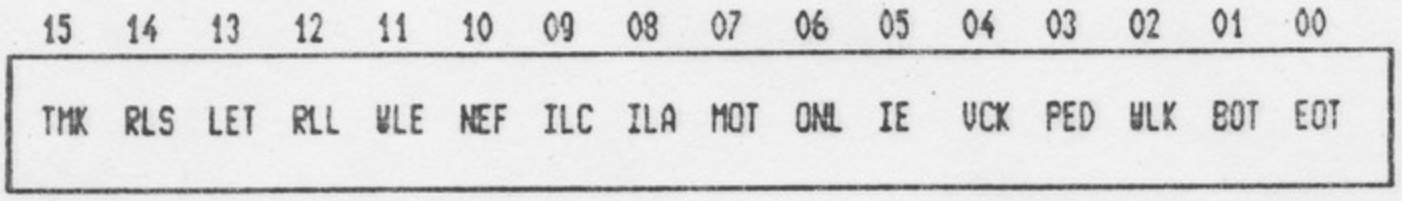
3.2.4.1 Residual Frame Count Register (RBPCR) -



Residual Frame Count - Bits <15:00>

This word contains the octal count of residual bytes, records, tape marks for read, space records and skip tape mark commands. The contents are meaningless for all other commands.

3.2.4.2 Extended Status Register Zero (XST0) -



See Table 1-1 for definition of Termination Class (TC) Codes.

Tape Mark Detected (TMK) - Bit 15

This bit is set when a tape mark is detected during a read, space, or skip command and as a result of the write tape mark or write tape mark retry commands. (Causes TC2.)

Record Length Short (RLS) - Bit 14

This bit indicates one of the following three cases. The record length was shorter than the byte count for a read operation. A space record operation encountered a tape mark or BOT before the position count was exhausted. Or, the third possibility, a skip tape marks command was terminated by encountering BOT or a double tape mark (if skip tape marks command is enabled, see LET) before exhausting the position counter. (Causes TC2.)

Logical End of Tape (LET) - Bit 13

This is set only on the skip tape marks command under two conditions: when either two contiguous tape marks are detected or when moving off BOT and the first record encountered is a tape mark. The setting of this bit will not occur unless this mode of termination is enabled through use of the set characteristics command. (Causes TC2.)

Record Length Long (RLL) - Bit 12

When set, this bit indicates that the record read was longer than

the byte count specified. (Causes TC3.)

Write Lock Error (WLE) - Bit 11

When set, a TC3 indicates that a write operation was issued but the mounted tape did not contain a write enable ring. When set, TC6 indicates the WRT LOCK switch was activated during write operation.

Non-Executable Function (NEF) - Bit 10

When set, this bit indicates that the command could not be executed due to one of the following conditions: The command specified reverse tape direction but the tape was already positioned at BOT. A motion command was issued without the clear volume check (CVC) bit being set while the volume check bit was set. A write command was issued when the tape did not contain a write enable ring [Write Lock Status (WLS)]. (Causes TC3.)

Illegal Command (ILC) - Bit 09

This bit is set when a command is issued and either its command field or its command mode field contains codes not supported by the transport. (Causes TC3.)

Illegal Address (ILA) - Bit 08

This bit is set if an address greater than 18 bits in length is loaded into TCDB Register or if that register overflows. (Causes TC3.)

Capstan is Moving (MOT) - Bit 07

When set, this bit indicates that the tape was moved during the previous operation. (Causes TC3.)

On-Line (ONL) - Bit 06

When set, this bit indicates that the transport is on-line and operable. It causes a TC1 on ATTN interrupt or a TC3 (non-executable) function if rejected because the transport was off-line.

Interrupt Enable (IE) - Bit 05

This bit reflects the state of the interrupt enable bit supplied on the last command.

Volume Check (VCK) - Bit 04

This bit is set when the transport changes state (on-line to off-line and vice versa). It is always set after initialization. (Causes TC3.)

Phase Encoded Transport (PED) - Bit 03

When set, this bit indicates that the transport is capable of reading and writing only 1600 bit/in phase encoded data. It should always be set.

Write Locked (WLK) - Bit 02

When set, this bit indicates that the mounted tape reel does not have a write enable ring installed. Therefore the tape is write protected. (Causes TC3 and TC6.)

Beginning of Tape (BOT) - Bit 01

When set, this bit indicates that the tape is positioned at the load point as denoted by the BOT refective strip on the tape. This causes TC2 if reversed in BOT, and TC3 if at BOT when a reverse command occurs.

End of Tape (EOT) - Bit 00

This bit is set whenever the tape is positioned at or beyond the EOT reflective strip. It is not reset until the tape passes over the EOT reflective strip in the reverse direction under program control. System initialization always resets this bit (status on read, TC2 on a write). Manually moving EOT mark over the EOT sensor will not set or reset the EOT bit.

3.2.4.3 Extended Status Register One (XST1) -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
DLT	0	COR	0	TIG	0	0	0	0	0	IPO	0	0	0	UNC	MTE

See Table 1-1 for Temination Class (TC) code definitions.

Data Late (DLT) -Bit 15

This bit is set when the I/O silo is full on a read or, empty on a write. The conditions occur whenever the Unibus latency exceeds the transport's data transfer rate for a significant number of transfers. (Causes TC4.)

Correctable Data (COR) - Bit 13

This bit is set if a single track error correction condition is detected during the execution of a read or write command.

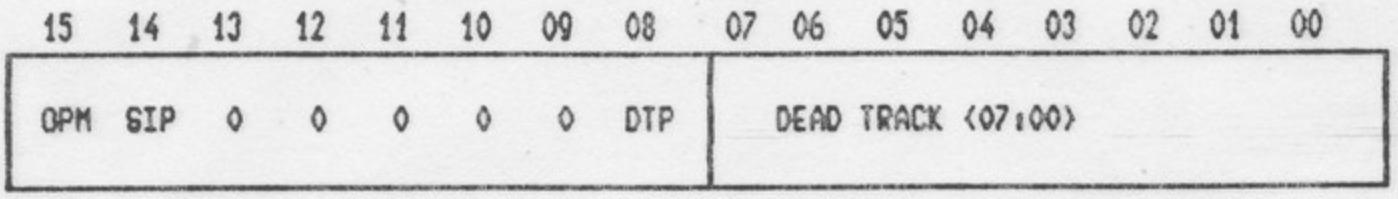
Uncorrectable Data (UNC) - Bit 01

This bit is set when a parity error occurs without a corresponding dead track indication.

Multitrack Error (MTE) Bit - 00

This bit is set if more than one dead track occurs in the preamble or in the data field. (Causes TC4 and TC5.)

3.2.4.4 Extended Status Register Two (XST2) -

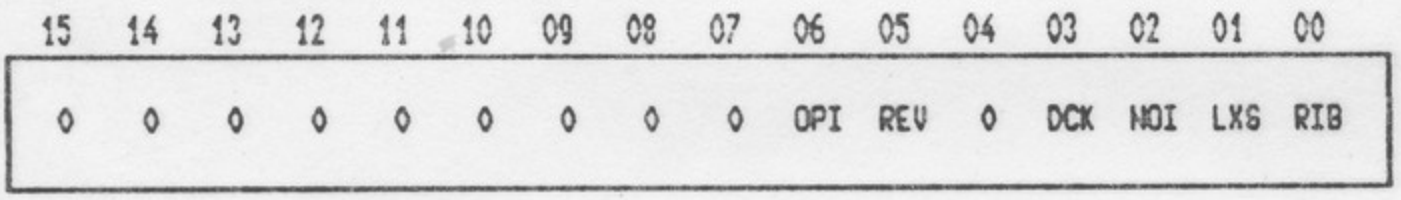


See Table 1-1 for Termination Class (TC) Code definitions.

Operation in Progress (OPM) - Bit 15

When set, this bit indicates that the tape was moved during the previous operation.

3.2.4.5 Extended Status Register Three (XST3) -



Operation Incomplete (OPI) - Bit 06

This bit is set when a read, space, or skip operation has moved 25 feet of tape without detecting any data on the tape. It is also set by a write command when the read head fails to see data transitions after four feet of tape. (Causes TC6.)

Reverse (REV) - Bit 05

This bit is set when the direction of current tape operation is reverse. For multifunction retry commands, if at least one of the commands is reverse, the bit is set.

Reverse Into BOT (RIB) - Bit 00

This bit is set when a read, space, skip, or reverse command already in progress encounters the BOT marker when moving tape in the reverse direction. Tape motion will be halted at BOT. (Causes TC2.)

3.3 PACKET PROCESSING

The packet protocol scheme allows each TS11 emulation (transport) on the transport to provide a large amount of status and error information to the CPU while taking up only two words of Unibus address space. The packet protocol also prevents the transport from updating the error and status information asynchronously, that is, while the CPU is reading the error and status information.

NOTE

This section is not intended to detail all aspects of packet protocol or packet processing. It is intended to illustrate how these concepts are implemented in the transport subsystem.

To allow each transport to take up only two words of address space, we allow the CPU to define a set of locations in memory. These locations (command buffers) are used to tell the transport what operation to perform. The CPU also defines a set of locations (message buffers) in memory where the transport will put the error and status information. The CPU must give both the command buffer address and message buffer address to the transport. The CPU gives the command buffer address to the transport on every command. (The CPU writes the address of the command packet into the TSDB of the transport.) The CPU gives the

message buffer address to the transport every time the CPU does a set characteristics command.

To prevent the transport from updating the message buffer while the CPU is reading that buffer, we have defined the concept of ownership. Both the command and message buffers can be owned. Each buffer may be owned by the transport or the CPU, but not by both simultaneously. Ownership of a buffer can only be transferred by the current owner.

There are four different combinations that transfer the ownership of the two buffers:

Command buffer - CPU to transport by the CPU;
Command buffer - transport to CPU by the transport;
Message buffer - CPU to transport by the CPU and
Message buffer - transport to the CPU by the transport.

The CPU transfers ownership of the command buffer to the transport by writing the address of the command packet into the TSDB. This write clears the TSSR subsystem ready (SSR) bit.

The transport transfers ownership of the command buffer to the CPU by setting the acknowlrdge (ACK) bit in the message buffer. When the transport outputs the message buffer, the transport sets SSR in the TSSR to indicate that the message is in the message buffer. If the message buffer does not contain the ACK bit, the CPU will know that the transport did not see the last command buffer and the CPU still owns the command buffer. The command may be reissued by the CPU.

The CPU transfers ownership of the message buffer to the transport by setting the ACK bit in the command buffer. If the command buffer does not contain the ACK bit, the transport will know that the CPU did not see the last message buffer and the transport still owns the message buffer. The transport outputs the TSSR again (with the SSR bit up) and interrupts (if IE is set) without sending out a message.

The transport transfers ownership of the message buffer to the CPU in one of two ways. The first way is used after the end of a command: the transport sets the SSR bit in the TSSR to indicate that the command is done (and interrupts if IE is set). The second way is used during an attention (ATTN). SSR will already

be up because an ATTN only happens when the transport is inactive. The transport clears SSR, outputs the message, then sets SSR again and interrupts (if IE set). Note that if the CPU writes the TSDB while the SSR is clear during an ATTN, the register modification refused (RMR) error bit will be set and that command will be ignored. The ATTN message will not have the ACK bit set since the transport does not own the command buffer. Note that RMR may set in this way on a bug free system because the CPU happened to try to perform a command at the same time the transport wanted to perform an ATTN. All other settings of the RMR indicate a software bug. (The CPU tried to do a command before the previous command was finished.) If the CPU command was lost because the transport was outputting an ATTN message, VOL CHK and INT ENB are not updated. If the CPU command was rejected (ilegal command, etc.), VOL CHK and INT ENB are updated to the start of the rejected command.

When the transport is initialized, the TSSR is updated. At this time we define both the command and message buffers as belonging to the CPU. When the CPU wants to do a command (the first one must be a set-characteristics to set up the message buffer address), the CPU writes the address of the command buffer into the TSDB of the transport. This command must have the ACK bit set to give ownership of the message buffer to the transport. At this point, the transport owns both the command and message buffers.

The transport will execute the set characteristics command and send out a message to the message buffer address with the ACK bit set; this indicates that the transport has recognized the command and is finished with the command buffer. The transport will then set SSR and interrupt (if IE is set). At this point, the CPU owns both the message and command buffers again.

As you can see, the ownership of both buffers transfers simultaneously from CPU to transport and then from transport to CPU.

Now consider the case where ATTNs are enabled by the proper characteristics mode word and the transport wants to do an ATTN. An ATTN will only occur when the transport is not active. If the CPU owns both the command and message buffers, the transport must queue up the ATTN and not do anything until the CPU releases the message buffer on the next command. So when the CPU executes the next command (with the ACK bit set), the transport will output

the ATTN message with the ACK bit zero; this indicates that the command was lost (except for the transfer of the message buffer ownership to the transport). The transport refuses to accept ownership of the command buffer. The CPU will then still own the command buffer (because the transport did not accept the command) and will also own the message buffer now filled with an ATTN message. If the CPU still wants to do the ignored command, the CPU must reissue the command (with the ACK bit set).

Now consider the case where the CPU wants to be notified of a change in status right away while the transport is inactive for a long period of time. To accomplish this, the transport must own the message buffer for that long period of time. Everything up to now has indicated that the transport gives up the message at the end of every command. The message buffer release command is a special command from the CPU. It tells the transport not to give ownership of the message buffer back to the CPU at the end of the command. The transport does not output a message at the end of the command but just outputs the TSSR (with the SSR bit set) and interrupts (if the proper characteristics mode word is set up). The transport then maintains ownership of the message buffer until an ATTN condition is seen. The transport then immediately clears SSR, outputs the message (with the ACK bit not set since the transport is not responding to a command), and then sets SSR and interrupts (if IE is set). At that time the system is back to the state of the CPU owning both buffers. Another ATTN will not be done until the CPU does a command with the ACK bit set to release ownership of the message buffer containing the ATTN message.

Suppose the CPU has done a message buffer release command and wants to do another command but has not received an ATTN from the transport (so that the transport still owns the message buffer from the message buffer release command). The CPU can do a command without the ACK bit set in the command buffer. At the time of the command, the CPU does not own the message buffer so the CPU cannot release the message buffer. If the CPU does set the ACK bit, nothing will happen (except the CPU might miss an ATTN if the transport was sending out an ATTN at the same time that the CPU was doing a command).

Message packet protocol may be violated if the transport gets an error (NXM, memory parity, serial bus parity error, or I/O silo parity error) during the reading in of the message packet. When

one of these errors occurs, the transport always sends out a failure message (because the packet is not reliable).

The system software should be written so it will not crash if the transport interrupts while the CPU is servicing another TSC01/11 interrupt. This may happen, but only if the transport should receive a fatal hardware error.

3.3.1 Command Packet/Header Word

Acknowledge - Bit 15

This bit is set when a command is issued and the CPU owns the message buffer. It informs the transport that the message buffer is now available for any pending or subsequent message packets. This passes ownership from the message buffer to the transport.

Device Dependent Bits/Field - Bits <14:12>

The following shows how these three bits are implemented:

Bit	Name	Definitions
14	CVC	Clear volume check
13	OPP	Opposite (reverse the execution sequence of the reread commands)
12	SWB	Swap bytes

Command Mode Field - Bits <11:08>

This bit acts as an extension to the command code and mode field and allows specification of extended device commands (seek, rewind, erase, write tape mark, etc.). Command code and mode field are detailed in Table 1-2.

Packet Format 1 Field - Bits <07:05>

The following two values are defined in this field.

Bit Values	Definition
000	One word header: interrupt disable
100	One word header: interrupt enable

Command Code Field - Bits <04:00>

Refer to Table 1-2 for definition of the three LS bits of the code.

Bits 03 and 04 of the command code field determine the format and length of command packets. The command packet formats and lengths are as follows.

Code Bits	Definition
00XXX	Four words (header, two word address, count)
01XXX	Two words (header, parameter word) or one word (header)

The swap byte bit in the command packet header word (bit 12) instructs the transport to alter the sequence of storing and retrieving bytes from the CPU's memory. When swap bytes equals one, an industry compatible sequence (beginning with an even byte) is used. When swap bytes equals zero, the swapping begins with an odd byte. (This is so only for data transferring; it is ignored otherwise.)

The following figures (Figures 1-1 and 1-2) indicate the memory positions for the bytes as they are read from or written on the tape. The bytes of data in the record block on tape are numbered starting at zero. Byte zero is always the data byte at the beginning of the block (that is, the part of the block that is closest to BOT).

NOTE: When reading in reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next to last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

FIGURE 1-1 BYTE SWAP SEQUENCE, FORWARD

swap bytes = 0
buffer address = 1000
byte count = 10(8)
block size = 10(8)bytes

1000	1	0
1002	3	2
1004	5	4
1006	7	6

swap bytes = 1
buffer address = 1000
byte count = 10(8)
block size = 10(8)bytes

1000	0	1
1002	2	3
1004	4	5
1006	6	7

swap bytes = 0
buffer address = 1001
byte count = 10(8)
block size = 10(8)bytes

1000	0	
1002	2	1
1004	4	3
1006	6	5
1010		7

swap bytes = 1
buffer address = 1001
byte count = 10(8)
block size = 10(8)bytes

1000		0
1002	1	2
1004	3	4
1006	5	6
1010	7	

FIGURE 1-2 BYTE SWAP SEQUENCE, REVERSE

```
swap bytes = 0
buffer address = 1000
byte count = 10(8)
block size = 10(8)bytes

1000 | 1 | 0 |
1002 | 3 | 2 |
1004 | 5 | 4 |
1006 | 7 | 6 |

swap bytes = 0
buffer address = 1001
byte count = 10(8)
block size = 10(8)bytes

1000 | 0 |   |
1002 | 2 | 1 |
1004 | 4 | 3 |
1006 | 6 | 5 |
1010 |   | 7 |

swap bytes = 0
buffer address = 1000
byte count = 7
block size = 7 bytes

1000 | 1 | 0 |
1002 | 3 | 2 |
1004 | 5 | 4 |
1006 |   | 6 |

swap bytes = 0
buffer address = 1001
byte count = 7
block size = 7 bytes

1000 | 0 |   |
1002 | 2 | 1 |
1004 | 4 | 3 |
1006 | 6 | 5 |

swap bytes = 1
buffer address = 1000
byte count = 10(8)
block size = 10(8)bytes

1000 | 0 | 1 |
1002 | 2 | 3 |
1004 | 4 | 5 |
1006 | 6 | 7 |

swap bytes = 1
buffer address = 1001
byte count = 10(8)
block size = 10(8)bytes

1000 |   | 0 |
1002 | 1 | 2 |
1004 | 3 | 4 |
1006 | 5 | 6 |
1010 | 7 |   |

swap bytes = 1
buffer address = 1000
byte count = 7
block size = 7 bytes

1000 | 0 | 1 |
1002 | 2 | 3 |
1004 | 4 | 5 |
1006 | 6 |   |

swap bytes = 1
buffer address = 1001
byte count = 7
block size = 7 bytes

1000 |   | 0 |
1002 | 1 | 2 |
1004 | 3 | 4 |
1006 | 5 | 6 |
```

3.3.2 Command Packet Examples

Examples of the command packets and operational programming notes used in the transport Subsystem are provided in this section. Refer to the figure and section number corresponding to the command packet example you are interested in.

NOTE: All four words of the command packet are always read in, even if the command takes only one word (rewind) or two words (space). Thus, the command packet must contain four words, and it must have good parity because the transport will reject the command packet on the basis of errors in the unused words.

3.3.2.1 Get Status Command -

NOTE: See message packet examples for data format

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.		MODE			FMT 1			COMMAND				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	1	1	1
NOT USED															

The get status command packet is illustrated above. This command causes an update of the five extended status registers in the message buffer area. However, after the end of any command, the transport hardware automatically updates the extended status registers. Therefore, this command need only be used when the transport has been left idle for some time or when a status register update is desired without performing a read, write or position tape command.

3.3.2.2 Read Command -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.		MODE			FMT 1				COMMAND			
ACK	CVC	OPP	SWB	X	X	X	X	IE	0	0	0	0	0	0	1
A15	LOW ORDER BUFFER ADDRESS														A00
0	HIGH ORDER BUFFER ADDRESS												0	A17	A16
BYTE COUNT (16 BIT POSITIVE NUMBER)															

The read command packet is illustrated above. There are four modes of operation: read forward, read reverse, reread previous, and reread next. In all cases a read operation is assumed to be for a record of known length. Therefore, the correct record byte count must be known. If the byte count is correct, normal termination occurs. If the record is shorter than the byte count, record length short (RLS) will set and a tape status alert (TSA) will be set. Also, any read operation that encounters a tape mark does not transfer any data. In this case tape mark (TMK) and record length short (RLS) are set and a tape status alert (TSA) termination occurs.

Read reverse operations which run into BOT cause Reverse Into BOT (RIB) to set and cause a tape status alert (TSA) termination. Tape motion will stop at BOT. Read reverse while at BOT will cause a function reject (NEF) status, with no tape motion.

NOTE: When reading reverse, the first data byte read is the last data byte of the sequence written. The read reverse command stores this first byte in the last buffer position; the next byte in the next to last buffer position, etc. This results in having data put in memory in the right order when reading the buffer sequentially.

3.3.2.3 Write Characteristics Command -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.			MODE			FMT 1				COMMAND		
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	0	1	0	0
A15						LOW ORDER CHARACTERISTIC DATA ADDRESS									A00
0						HIGH ORDER CHARACTERISTIC DATA ADDRESS							0	A17	A16
BYTE COUNT (16 BIT POSITIVE NUMBER)															

Message packet example

TSC01/11 TAPE COUPLER
PACKET PROCESSING

A15							LOW ORDER MESSAGE BUFFER ADDRESS								A00
0							HIGH ORDER MESSAGE BUFFER ADDRESS						0	A17	A16
LENGTH OF MESSAGE BUFFER (AT LEAST 14 BYTES LONG)															
0	0	0	0	0	0	0	0	ESB	ENB	EAI	ERI	0	0	0	0

The figure above illustrates the write characteristics command packet. Its objective is to inform the transport Subsystem of the location and size of the message buffer in CPU memory space. The message buffer must be at least seven contiguous words long and must begin on a word boundary.

The write characteristics command also transfers a characteristics mode byte to the transport. This word causes specific actions for certain operational modes. The bits for this word are defined below.

If a good message buffer address has not been loaded with a write characteristics command, the need buffer address (NBA) bit in the TSSR register will be set.

Enable Skip Tape Marks Stop (ESS) - Bit 07

When this bit is set, it instructs the transport to stop during a skip tape mark command when a double tape mark (two contiguous tape marks) has been detected. In the default setting of 0, the skip tape marks command will terminate only on tape mark count exhausted or if it runs into BOT.

(ENB) - Bit 06

This bit is only meaningful if the ESS bit is set. If the transport is at BOT when a skip tape marks command is issued and the first record seen is a tape mark, then the transport will set LET and stop after the first tape mark. If the bit is clear, the transport would not set LET but count the tape mark and continue.

Enable Attention Interrupts (EAI) - Bit 05

When this bit is a zero, attention conditions, such as off-line, on-line, and microdiagnostic failure, will not result in interrupts to the CPU. If set to a one, interrupts will be generated.

NOTE: transport must own the message buffer, via message buffer release, to set attention interrupts.

Enable Message Buffer Release Interrupts (ERI) - Bit 04

If this bit is zero, interrupts will not be generated when a message buffer release command is received by the transport.

Upon recognition of the command, only subsystem ready (SSR) will be reasserted. If ERI is a one, an interrupt will be generated.

3.3.2.4 Write Command -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.		MODE			FMT 1			COMMAND				
ACK	CVC	0	SWB	X	X	X	X	IE	0	0	0	0	1	0	1
A15	LOW ORDER BUFFER ADDRESS														A00
0	HIGH ORDER BUFFER ADDRESS									0	A17				A16
BYTE COUNT (16 BIT POSITIVE NUMBER)															

The figure above illustrates the write command packet. There are two modes: write data and write data retry (space reverse, erase, write data). Each operation is straightforward and designed to transfer data onto tape in the forward direction only.

If a write command is executed at or beyond the EOT marker a tape status alert (TSA) termination will occur. EOT will remain set until passed in the reverse direction or a subsystem initialize.

If a write command is executed anywhere and the identification burst (IDB) was previously written bad or was not found when it left BOT, then density check (DCK) is set and tape position lost termination occurs.

3.3.2.5 Position Command -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.			MODE		FMT 1				COMMAND			
ACK	CUC	0	0	X	X	X	X	IE	0	0	0	1	0	0	0
TAPE MARK/RECORD COUNT (16 BIT POSITIVE NUMBER)															

The position command packet is illustrated above. This command causes tape to space records forward or reverse, skip tape marks forward or reverse, and to rewind to BOT. An exact tape mark/record count must be the second word of the packet for skip tape mark and space record commands.

A space records operation automatically terminates when a tape mark is traversed. Also, record length short (RLS) is set if the record count was not decremented to zero.

A skip tape marks command terminates when it encounters a double Tape mark and the enable skip stop mode is specified (ESS bit set) in the characteristics word. Termination will also occur if a tape mark is the first record off BOT and ESS and ENB bits are set in the characteristics word. Record length short (RLS) is set if the record count is not decremented to zero.

A space records reverse or skip tape marks reverse, which runs into BOT, sets reverse into BOT (RIB) and causes a tape status alert termination.

When a rewind command is issued, the interrupt will not occur until the tape reaches BOT in the forward direction and has begun

to decelerate. Due to tape speed during rewind, the transport overshoots BOT in the reverse direction and then moves the tape forward until BOT is located before terminating the operation. Normal termination will be indicated if the operation is completed without incident. If the tape is already at BOT, the rewind will still be done to make sure the tape is positioned properly.

NOTE: If the tape is positioned between BOT and the first record and you do a space reverse or skip reverse, RIB wil set and the residual frame count equals the specified count in the original command.

3.3.2.6 Format Command -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.			MODE			FMT 1				COMMAND		
ACK	CVC	0	0	X	X	X	X	IE	0	0	0	1	0	0	1
NOT USED															

The above figure illustrates the format command packet. This command can write a tape mark, rewrite a tape mark, and erase tape. In all cases, executing a format command at our beyond OT will cause a tape status alert (TSA) termination. The EOT bit will remain set until passed in the reverse direction. A subsystem initialize can also reset the EOT bit. Also, any format command executed with density check (DCK) set will cause a tape position lost termination.

Density check is set when a invalid identification burst (IDB) is read off BOT. This occurs in a read after write mode within the first three inches of tape and is transparent to the user's operation.

The erase command will cause three inches of tape to be erased. This length is controlled automatically by the transport hardware. Successive erase commands can be used to erase more than three inches (in three inch increments).

3.3.2.7 Control Command -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.		MODE			FMT 1			COMMAND				
ACK	CUC	0	0	X	X	X	X	IE	0	0	0	1	0	1	0
NOT USED															

The figure above illustrates the control command packet. The three modes of operation are message buffer release, unload, and clean. The message buffer release command, when executed with the ACK bit set, allows the transport to own the message buffer so it can update the status in the status in the message buffer area on an ATTN. This is beneficial when the operating system is processing data in other areas not concerned with operating the transport Subsystem and the host wants to know the current transport status.

The unload command is designed to rewind tape completely onto the supply reel. When the command is executed, termination occurs immediately; an interrupt will occur if IE is set.

The clean tape command moves ten inches of tape over the tape cleaners and returns it to the original position. Successive clean tape commands are not recommended since the tape may creep outside the interrecord gap (IRG) margins. Also, the clean tape command does not recognize BOT. (That is, you can clean tape and reverse past BOT and back again without setting status bits.)

3.3.2.8 Initialize Command -

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	DEV.		DEP.		MODE			FNT 1			COMMAND				
ACK	CVC	0	0	0	0	0	0	IE	0	0	0	1	0	1	1
NOT USED															

The initialize command packet is illustrated above. This command is not very useful, but is included for compatibility with packet protocol. A transport initialize can be done by a write to the TSSR, as this action does not need a command packet.

The transport initialize command is a no-op. It results in a message update, just like a get status, if there are no microdiagnostic or runaway errors. However, if errors are displayed, the command does the same thing as a write to the TSSR. Section 3.1.3 contains TSSR details.

3.3.3 Message Packet Header Word

Acknowledge - Bit 15

This bit is used by the transport to inform the CPU that the command buffer is now available for any pending or subsequent command packets. On an ATTN message, this bit will not be set since the transport does not own the command buffer.

Reserved - Bits <14:12>

These bits are reserved for future expansion.

Class Code Field - Bits <11:08>

These bits define the class of failures found in the rest of the message buffer.

MSG Type	Class Value	Definition
ATTN	0000	On-or off-line
FAIL	0001	Other (ILC,ILA,NBA)
FAIL	0010	Write lock error or non-executable function

Packet Format 1 Field - Bits <07:05>

The single value supported by the TS12 is as follows.

Value	Definition
000	One word header

Message Code - Bits <04:00>

Term Class	Value	Definition
0,2	10000	End
3	10001	Fail
4,5,6,7	10010	Error
1	10011	Attention

3.3.4 Message Packet Example

All message packets are identical. Each message packet contains the message packet header word just described, plus a data length field word and the five extended status registers. The figure below illustrates the message packet format.

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
CTL	RESERVED			CLASS CODE				PACKET FMT.			MESSAGE CODE				
ACK	0	0	0	0	0	C	C	0	0	0	1	M	M	M	M

3.4 OPERATIONAL INFORMATION

The following information considers the operation and programming requirements of the transport Subsystem.

3.4.1 Unibus Registers

Each transport has two Unibus word locations used as device registers. The base address, when written to, is the data buffer register (TSDB). When read, it is the bus address register (TSBA). The second device register (base address + 2) is the status register (TSSR). Writing to the TSSR causes a subsystem initialize command, and reading the TSSR reads device status.

The TSDB register is the only register written to during normal operations. DATO or word access must be used to properly write command pointers to the TSDB. DATOB or byte access to the TSDB causes maintenance functions.

Commands are not written to the transport's Unibus registers. Instead, command pointers, which point to a command packet

somewhere in CPU memory space, are written to the TSDB register. The command pointer is used by the transport to retrieve the words in the command packet. The words of the command packet tell the transport the function to be performed. They also contain any function parameters such as bus address, byte count, record count, and modifier flags.

3.4.2 Command and Message Packets

Comand packets must reside on modulo - 4 address boundaries within CPU memory space. This means the starting address of the packet must be devisible by 4 (that is, octal 00, 04, 10, 14, etc.).

All four words of a command packet must exist and have good memory parity, even if all four words are not used by a command. (For instance, rewind uses only one word.)

Message packets are issued by the subsystem and are deposited into the CPU's memory space. Controlled operation of the transport requires that it be supplied a message buffer address on write characteristics command. The five extended status registers are stored in this message buffer area. The END message packet, which results at the end of any command, contains these extended status words.

3.4.3 Special Conditions and Errors

Table 1-3 includes the meanings of the binary values within the termination class code field in the TSSR register.

Table 1-3
Termination Class Codes

TC2-0 Value	Msg Type	Offset	Meaning
0	END	00	Normal termination: This bit indicates the operation was completed without incident.
1	ATTN	02	Attention Condition: This code

			indicates that the transport hasundergone a status change going off-line, coming on-line or a microdiagnostic failure.
2	END	04	Tape Status Alert: This bit indicates a status condition has been encountered that has significance to the program. Bits of interest include TMK, EOT, RLS, and RLL.
3	FAIL	06	Function Reject: This bit indicates the specified function was not initiated. Bits of interest include OFL, VCK, BOT, WLE, ILC and ILA.
4	ERR	10	Recoverable Error: This bit indicates tape position is one record beyond what its position was when the function was initiated. Suggested recovery procedure is to log the error and issue the appropriate retry command.
5	ERR	12	Recoverable Error: This bit indicates tape position has not changed.Suggested recovery procedure is to log the error and reissue the original command.
6	ERR	14	Unrecoverable Error: This bit indicates tape position has been lost. No valid recovery procedures exist unless the tape has labels or sequence numbers.
7	ATTN/ ERR	16	Fatal Subsystem Error: This bit indicates the subsystem is incapable of properly performing commands or at least that

the subsystem's integrity
is seriously questionable.

3.4.4 Status Error Handling Notes

TSSR error bits, other than the fatal class, termination class, and SC bits, are cleared by loading a command pointer into the TSDB register. SC is reset if it is due to a TSSR error (UPE,SPE,RMR, or NXM). Extended status error bits are cleared after the END message is sent.

All commands (even get status command) clear the XSTAT error bits; except XSTAT3 bits 15 through 08 (microdiagnostic error code) and bit LXS are not cleared.

If a density check condition is detected during a read, space, or skip function, the DCK bit is set, but the operation is not stopped. If DCK is the only status bit set during the operation, normal termination is reported. This allows tapes with good data but bad density check areas to be read. If a wrong density tape has been mounted, other errors will be reported and the operation will stop. Note that if only the density check area is bad, the density check indicator on the transport's operator panel lights, even though the data records might be the correct density. The DCK indicator will remain lit until BOT is encountered again or until a subsystem initialize is performed. Note that if you can begin reading a tape, get a density check condition with no other errors, then append to the tape; the write will get a termination class code of 6. This indicates that the tape position is lost because density check will remain set. The whole tape should be copied over so that transports depending on the IDB will be able to read the tape.

A command is not responded to while another command is in progress (result is RMR), except in the following cases.

1. A DATO (word access) to the TSSR (subsystem initialize) brings any operation in progress to an immediate halt. All subsystem parameters which had been in the subsystem's memory (VCK reset, EOT, etc) are erased. Also, if the on-line switch is ON, the

transport performs an auto-load sequence and positions the tape at BOT.

2. The transport responds to any nontape motion command while performing a rewind unload (while the transport is off-line) because SSR is still up.

The transport also responds to any nontape motion commands (get status, transport initialize, set characteristics, and message buffer release) when off-line, except when in maintenance mode. (The subsystem ready command, SSR, is not asserted in this case and results in RMR.)

The following failures can occur without resulting in an interrupt, even though the specified command had interrupt enable set.

SPE - The possibility exists that the transport cannot transfer valid data or command information via the serial bus to the transport. In this case the SC, TC2, TC1, and TC0 bits are not valid either.

NXM,UPE,BPE - They might occur before the interrupt enable bit is fetched as part of the command packet.

CHAPTER 4

INSTALLATION

4.1 OWERVIEV

This section decsribes step-by-step procedure for installation of the TSC01/11 Magnetic Tape Coupler in a PDP-11 or VAX-11 CPU System.

4.2 INSPECTION

After unpacking the TSC01/11 tape coupler, visually inspect the entire assembly for bent or broken connector pins, damaged components, or other visual evidence of physical damage.

4.3 SLOT SELECTION

The coupler may be placed in any SPC slot along the Unibus without regard to NPR priority.

4.4 NPG SIGNAL JUMPER

The NPG signal between pins CA1 and CB1 on the selected backplane slot must be removed so that the NPG signal passes through the coupler.

4.5 PHYSICAL INSTALLATION

The coupler board should be plugged into connectors C, D, E, and F of the Unibus backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with computer power OFF to avoid possible damage to the circuitry. Be shure that the board is seated properly in the throat of the connector before attempting to install the board.

4.6 CABLING

The TSC01/11 interfaces to the drives via two industry-standard 50-wire cables. List of I/O signals onto two coupler's connectors is given in the appendix.

4.7 ADDRESS SELECTION

The TSC01/11 allows the user to select one of four address ranges. Each range includes starting addresses for four emulations (transports). The addresses within each range are contiguous.

The standard address range includes the CSR addresses fixed for TS11 type devices under VMS and other DEC operating systems. The three alternate ranges are not normally associated with the TS11. If one of the alternate ranges is selected, the autoconfigure utility will not locate or properly identify the device. In that case, the manual connect command can be used to configure the system.

One of four avaliable ddress ranges of TSC01/11 is selected by combining jumpers W7 and W8 as shown in Table 4-1.

Table 4-1
Unibus Starting Address

Component side look of the W7 jumper:

W7 A-B	W8	W7 B-C	Unibus Starting Address
OUT	OUT	IN	776300
IN	OUT	OUT	772520 (Standard address)
OUT	IN	IN	777460
IN	IN	OUT	772440

4.7.1 Coupler Address Selection

The DEC TS11 tape subsystem consists of one tape transport interfaced to the Unibus by a coupler. Each TS11 requires two Unibus addresses, one for each of its registers. The TSC01/11, which can support up to four individual tape transports, thus emulates four TS11 subsystems. Consequently, each transport interfaced to the sytem by the TSC01/11 is represented by a unique set of Unibus registers. There is a direct relationship between a transport's unit number and the Unibus base address for the subsystem it represents. The relationship between the transports and their addresses is depicted in Table 4-2.

Up to four tape transports may be daisy chained to one TSC01/11. Each tape transport must be assigned a unique device number in the range 0 to 3. The address assigned to the transport determines its Unibus address and device name (see Table 4-2).

Table 4-2
Individual Transport Addressing And Enabling

Transport Number	Unibus Address	Device Name	Enabling Jumper
0	Starting + 0	MS0	W9 (OUT=ENABLE)
1	Starting + 4	MS1	W10 (OUT=ENABLE)
2	Starting +10	MS2	W11 (OUT=ENABLE)
3	Starting +14	MS3	W12 (OUT=ENABLE)

4.7.2 Individual Transport Enabling
Each transport that is interfaced to the Unibus using the TSC01/11 must be individually enabled using jumpers W9 through W12.

Table 4-2 shows the relationship of the transport to its Unibus address and the jumper which enables it. This feature is useful if a DEC TS11 is already installed in the CPU at the standard Unibus starting address. It is desirable to place the second tape transport (the Delta emulation) at the next available bus address. This is done by selecting the standard Unibus address range on the TSC01/11, assigning the new transport a unit number of 1 and positioning W10 OUT. The other three enabling jumpers (W9, W11 and W12) are left IN to disable those Unibus addresses.

The tape transport's unit number must be set to correspond to the Unibus address required. That is, if an address of 772524 is required, the transport address would be set to one and jumper W10 would be OUT.

4.7.3 Interrupt Vector Address
Each tape unit must have an individual interrupt vector address. The TS11 is assigned one fixed interrupt vector (224) under VMS and other DEC operating systems. Vectors required for additional are assigned from floating vector address space.

The vector address is selected by 8-pole switch (SW2).

When SW2-8 is open (OFF), the address for unit zero is selected by switches SW2-1 through SW2-8. The vector addresses for units 0-3 are contiguous. Each address falls four words from the one before it. For example, if 300 is selected as the vector address for unit 0, the vector address for unit 1 will be 304, the address for unit 2 will be 310, and the address for unit 3 will be 314.

With SW2-8 closed (ON), the standard vector address of 224 is selected for unit 0. The addresses for units 1-3 are contiguous and their starting point is selected as described above. Unit one will be in the same relationship to the switch setting as previousely described; that is, the switch setting plus four. Remember, that the vector for unit 0 is 224 regardless of the switch settings with SW2-8 closed (ON).

Table 4-3 shows the relationship of SW2-1 through SW2-7 to the Unibus vector address bits they control.

Table 4-3
Vector Address

Octal	2	2	4
Binary	0 1 0	0 1 0	1 X X
Address Bit	08 07 06	05 04 03	02 01 00
Switch Setting	ON OFF ON	ON OFF ON	OFF X X
Switch SW2-	7 6 5	4 3 2	1 X X

An example of vector address selection is given below. The example is for four drives using contiguous vectors, starting at 244.

Unit	CSR Address	Vector	Switch SW2 Setting 1 2 3 4 5 6 7
1	772520	224	O C O C C O C
2	772524	230	
3	772530	234	
4	772534	240	

C - closed (ON)
O - open (OFF)

4.7.4 Optional Switches

The 4-pole PIANO switch (SW1) is used for diagnostic purposes.

4.7.4.1 Delayed power-up option -

PIANO switch SW1-1 allows TSC01/11 to execute long power-up sequence (app. 1 sec after power-up). When enabled (ON) the power-up sequence will take up to 1 sec. othervise the power-up sequence will take only a few miliseconds.

4.7.4.2 Loop micro-diagnostic option -

PIANO switch SW1-2 allows selection of a constant power-up diagnostic mode. When enabled (ON) the TSC01/11 will perform diagnostic tests constantly upon power-up.

4.7.4.3 Run/Reset Option -

PIANO swich SW1-4 allows selection of the Run/Reset option. When enabled (ON), normal running of tape transport is halted, the TSC01/11 coupler is reset and initialized, and the tape on the tape transport is rewound to the BOT position.

4.8 TESTING

Testing is performed by the Self-Test routine in the TSC01/11 tape coupler and by running separate diagnostic programs.

4.8.1 Self-Test

When power is applied to the CPU, the coupler will automatically execute a bulit-in self-test. This self-test is executed with every bus INIT. If the self-test has been executed successfully, the Ready LED (CR3) will be ON. If the coupler did not pass its self-test a LED combination below indicates which test failed:

Ready CR3	Busy CR2	Wait CR1	Meaning
OFF	OFF	ON	Sequencer test failed
OFF	ON	OFF	Processor test failed
OFF	ON	ON	RAM test failed
ON	OFF	ON	Flag test failed
ON	ON	OFF	Test input failed

4.8.2 Diagnostics

The diagnostic test routines used with the TSC01/11 tape coupler depend on whether the CPU for the system is PDP-11 or VAX-11.

4.8.2.1 PDP-11 Diagnostics -

The dec TS11 should be run. Only the Controller Repair Diagnostic (ZTSI, runs first three test with a minor patch) and the Data Reliability Exerciser (ZTSH) need be run. The diagnostics can be loaded from an XXDP media.

On Unibus systems the naming convention for multiple TS11s is as follows:

a. Unit zero =MS0
b. Unit one =MS1
c. Unit two =MS2
d. Unit three =MS3

The patch that needs to be applied to ZTSI is:

Location	Is	Should Be
2122	12	3

4.8.2.2 VAX-11 Diagnostics -

If the TSC01/11 tape coupler is installed in a VAX-11 CPU, the VAX diagnostic should be used. The Data Reliability (EVMAA) and the TS11 Repair Diagnostic (EVMAD) are the only two diagnostic that need to be run.

NOTE

Subtest 2 of EVMAA reports two data compare errors when running off-line on a VAX-11/780 CPU. This error report is normal, even for DEC TS11 tape coupler. These errors are not reported if EVMAA is run on-line.

The TSC01/11 does not run tests 5 through 10, 15, 16, and 18 of EVMAD.

The VAX naming convention is defined in the following list:

a. Unit zero =MSA0
b. Unit one =MSB0
c. Unit two =MSC0
d. Unit three =MSD0

CHAPTER 5

TROUBLESHOOTING

5.1 PREVENTIVE MAINTENANCE

There are no adjustments or calibrations required in servicing the TSC01/11 tape coupler. IDC recomends the diagnostic software programs be used in the system checkout. The diagnostic programs should be run at regularly scheduled intervals to verify correct system operation.

NOTE

When any circut component has been replaced, the diagnostics should be run and all pertinent circuit characteristics should be checked before the system is returned to normal operation.

5.2 FAULT ISOLATION GUIDE

Table 5-1 is a Fault Isolation Guide that should be used as a diagnostic aid for the isolation of faults in the TC13 tape coupler system. It lists possible symptoms, probable cause of the malfunction, and corrective action.

TSC01/11 TAPE COUPLER
FAULT ISOLATION GUIDE

Table 5-1. TSC01/11 Tape Coupler Fault Isolation Guide

Symptom	Probabe Couse	Remedy
Cpu powered up, REDY LED does not lit.	Self-Test failure	Verify TSC01/11 tape PCBA is properly seated in CPU backplane. Also check to make shure SW1-4 is OFF. Defective unit.
Data transfer operation attempted but ACTIVITY/BUS LED not lit.	Cable for control lines or data lines reversed.	Check cable connetions.
	Interface cables to/from addressed not connected.	Connect cables to/from addressed tape transport.
	Addressed tape transport does not have Ready status.	Perform operations on tape transport that are needed to produce Ready (On-Line) status.
	Wrong CSR device address coded in configuraton DIP switches.	Encode correct address in configuration DIP switch pack.
Unable to interrupt CPU	Wrong Interrupt Vector Address coded in configuration DIP switch pack	Encode correct Interrupt Vector Address in configuration DIP switch pack

APPENDIX A

TSC01/11 OPTION SWITCHES

This appendix lists switch settings and functions.

The follwing is a list of factory settings:

- One transport is enabled (MS0)
- Starting CSR address is set to 1772520
- Interrupt Vector is set to 224
- Long (delayed) power-up is selected (SW1-1)

Table A-1 Tape Coupler Factory Switch Settings

Switch	Setting	Switch	Setting
SW1-1	OFF	SW2-1	OFF
SW1-2	OFF	SW2-2	OFF
SW1-3	OFF	SW2-3	OFF
SW1-4	ON	SW2-4	OFF
		SW2-5	OFF
		SW2-6	OFF
		SW2-7	OFF
		SW2-8	ON

Jumpers W7(A-B) IN, W10,W11,W12 IN.

Table A-2 SW1 Option Switch Settings

Switch	Open	Closed	Function
SW1-1	Normal	Long	Power-up delay
SW1-2	-	-	-
SW1-3	Disable	Enable	Micro diagnostic loop
SW1-4	Run	Reset	TSC01/11 reset

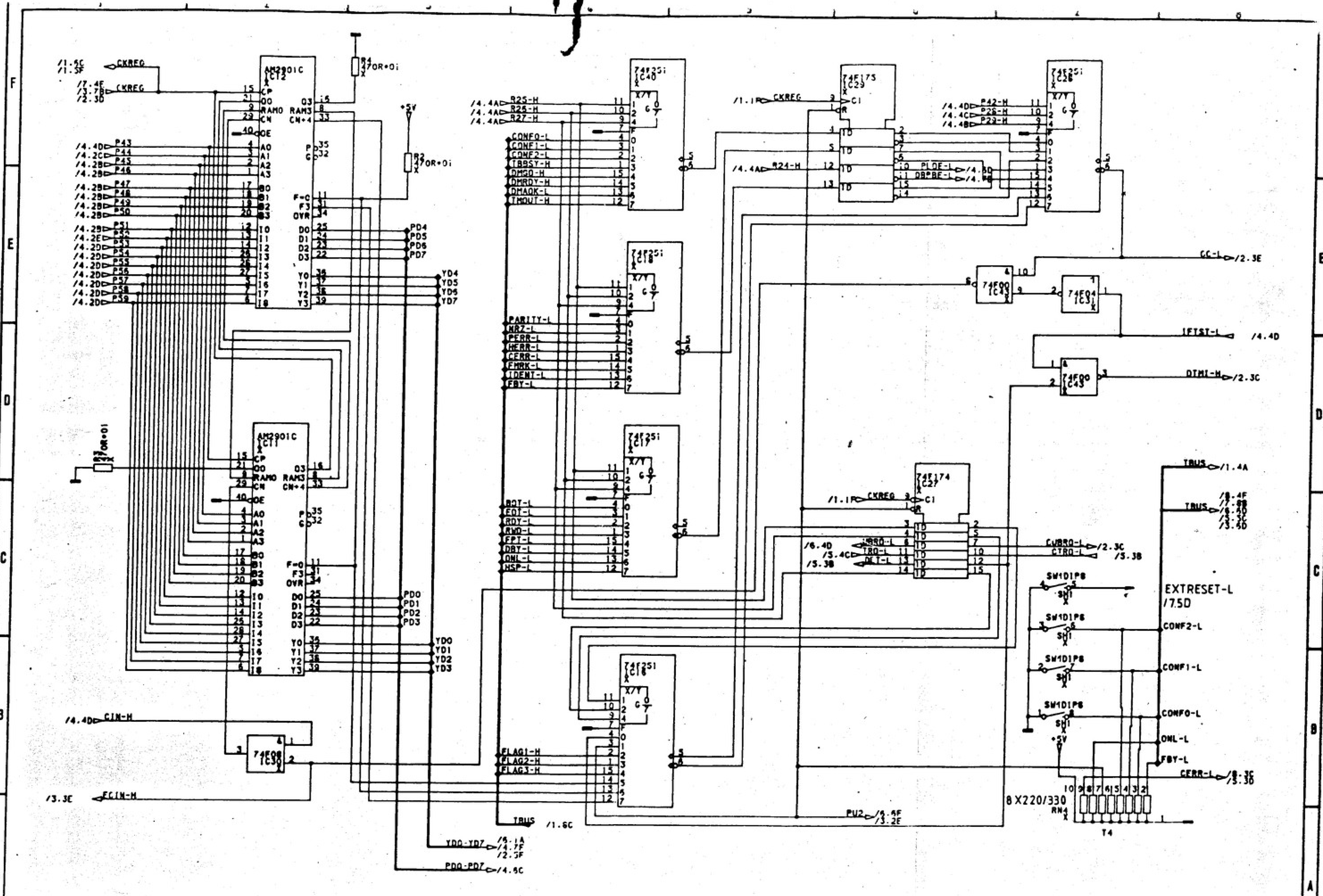
Table A-3 SW2 Option Switch Settings

Switch	Open	Closed	Function
SW2-1	Zero	One	Vector Address bit 2
SW2-2	Zero	One	Vector Address bit 3
SW2-3	Zero	One	Vector Address bit 4
SW2-4	Zero	One	Vector Address bit 5
SW2-5	Zero	One	Vector Address bit 6
SW2-6	Zero	One	Vector Address bit 7
SW2-7	Zero	One	Vector Address bit 8
SW2-8		224	Unit zero vector

TSC01/11 TAPE COUPLER

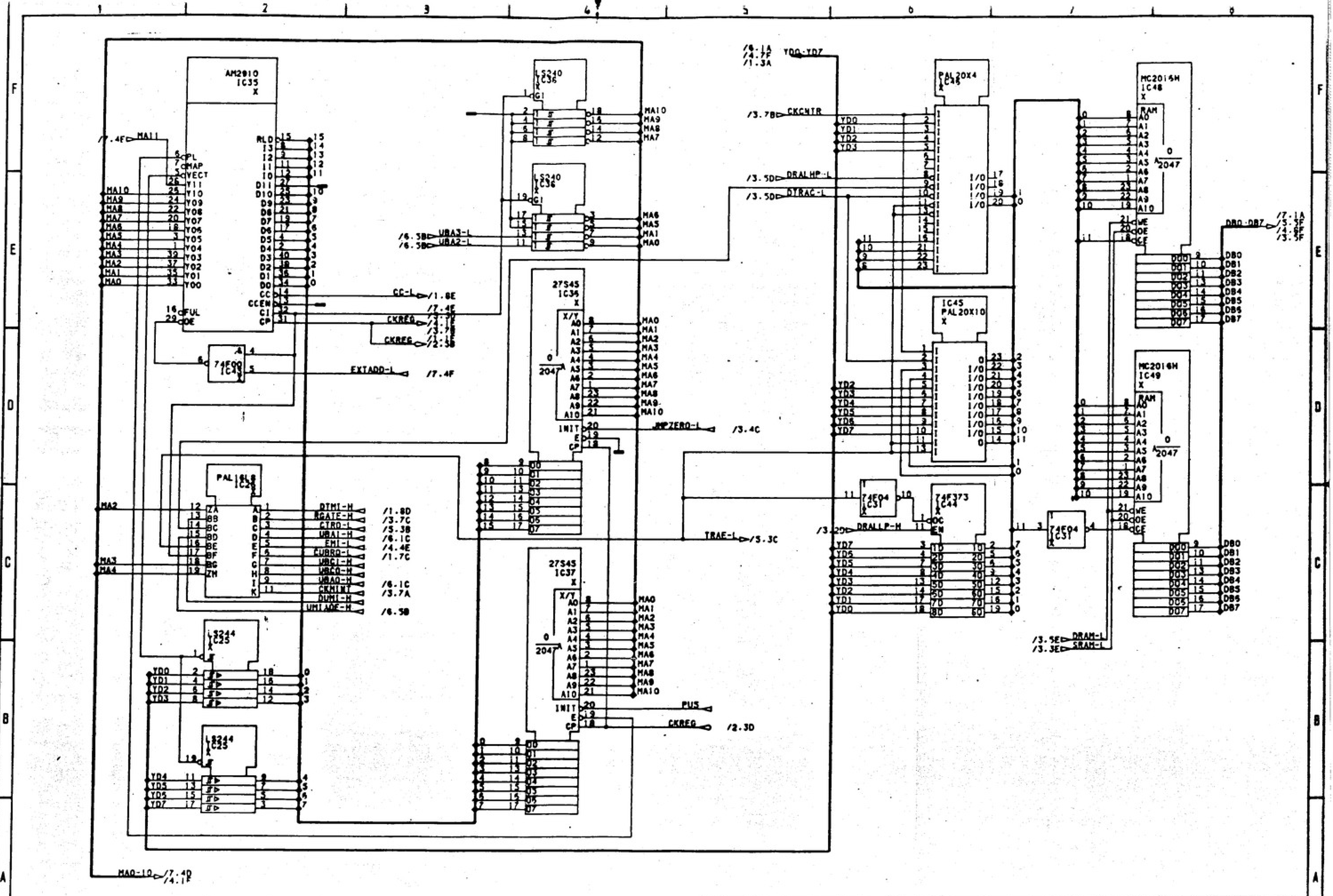
Table A-4 Jumpers

Jumper	In	Out	Function
W7,W8	-	-	Address selection see Table 4-1.
W9	Disable	Enable	Enable Tape transport 0
W10	Disable	Enable	Enable Tape transport 1
W11	Disable	Enable	Enable Tape transport 2
W12	Disable	Enable	Enable Tape transport 3



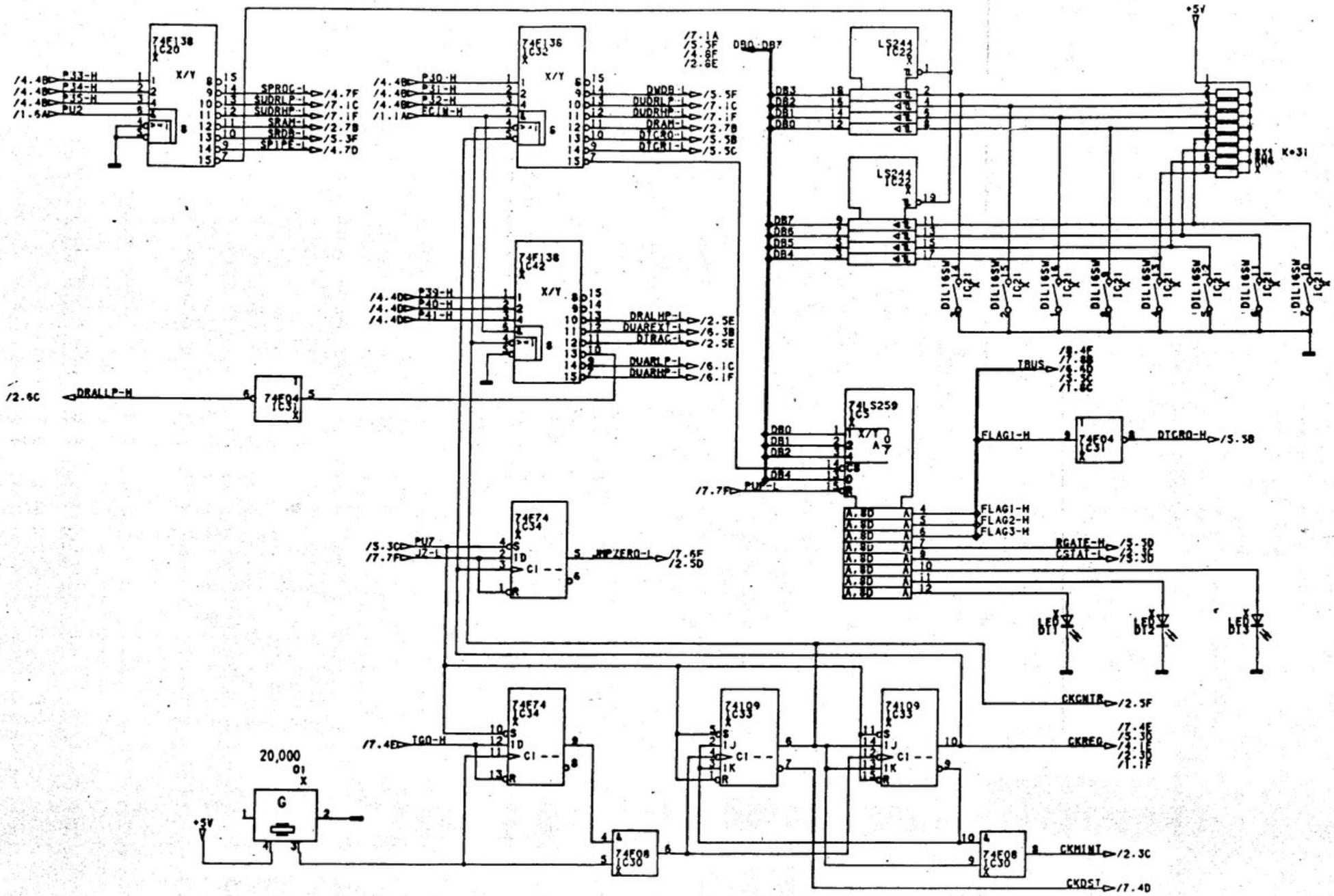
Izdaja						List	Stran	J	K	Identifikacijska številka
Št. obvestila						2				50403044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.				TSC01/11 L1		Arhiv				Namesto identifikacijska številka: 3263004 4

Obr. 42



Izdaja							List	Stran	J	K	Identifikacijska številka dok.
Št. obvestila							3				50403044
IskraDelta proizvodnja računalniških sistemov in inženiring, p.o.				TSC01/11 L2			Arhiv				Namesto identifikacijske številke 32630044

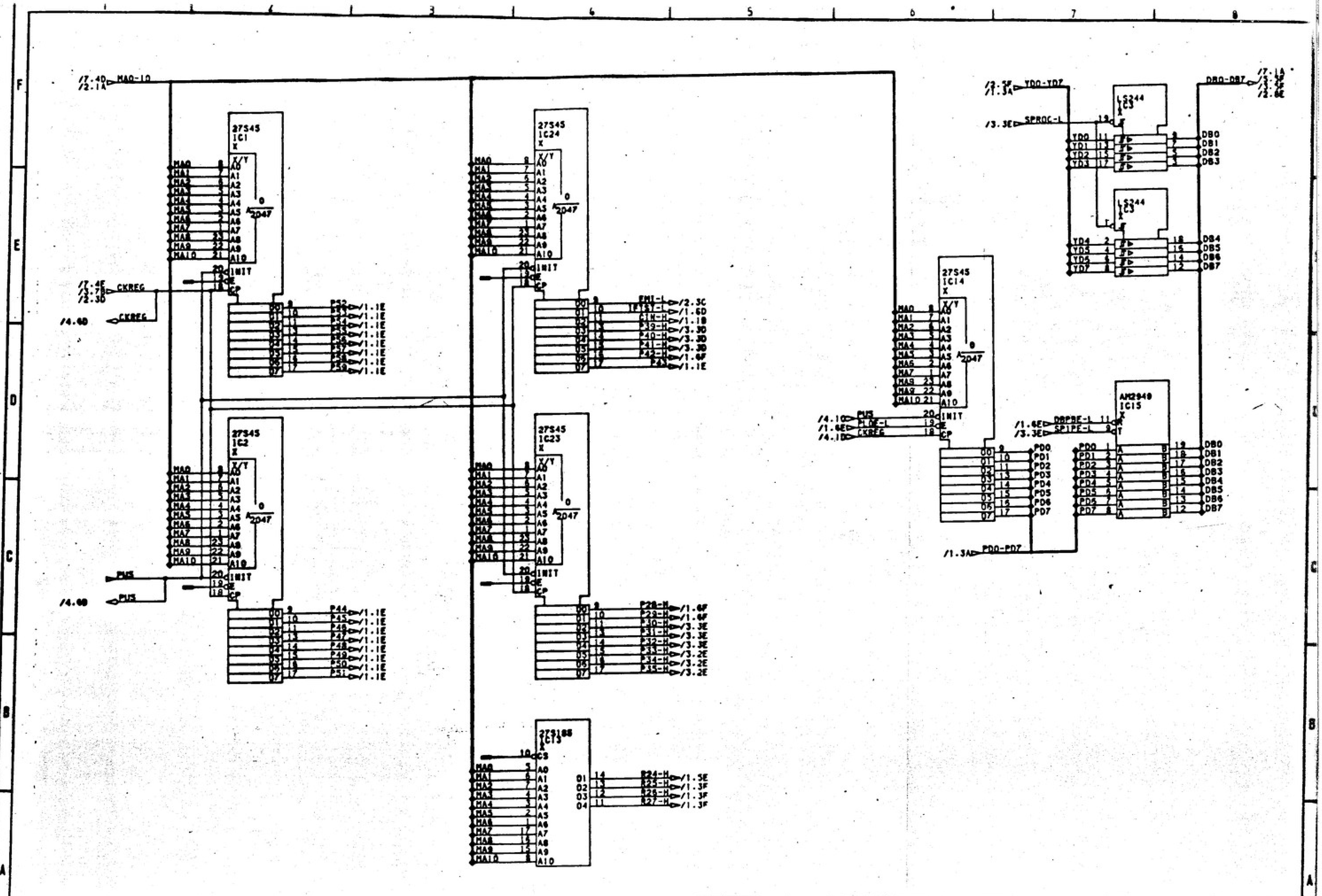
Obr. 42



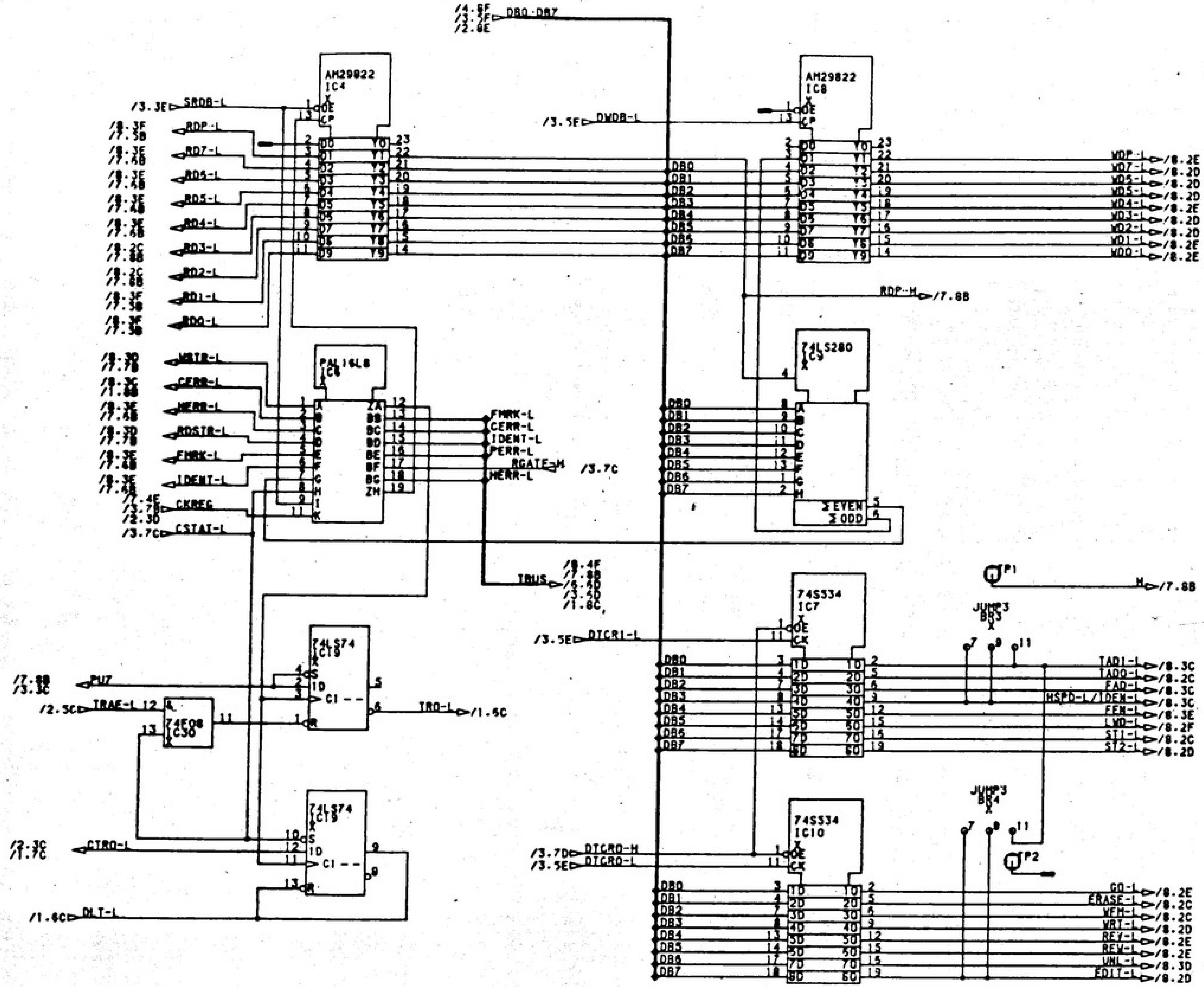
Izdaja							List	Strani	J	K	Identifikacijska številka dela:
Št. obvestila							4				50403044
Iskra Delta proizvodnja računalniških sistemov in inženiring, p.o.						TSC01/11 L3	Arhiv				Namesto identifikacijske številke: 32630044

Prenos tretjim osebam in uporaba v nedovoljene namene sta prepovedana.

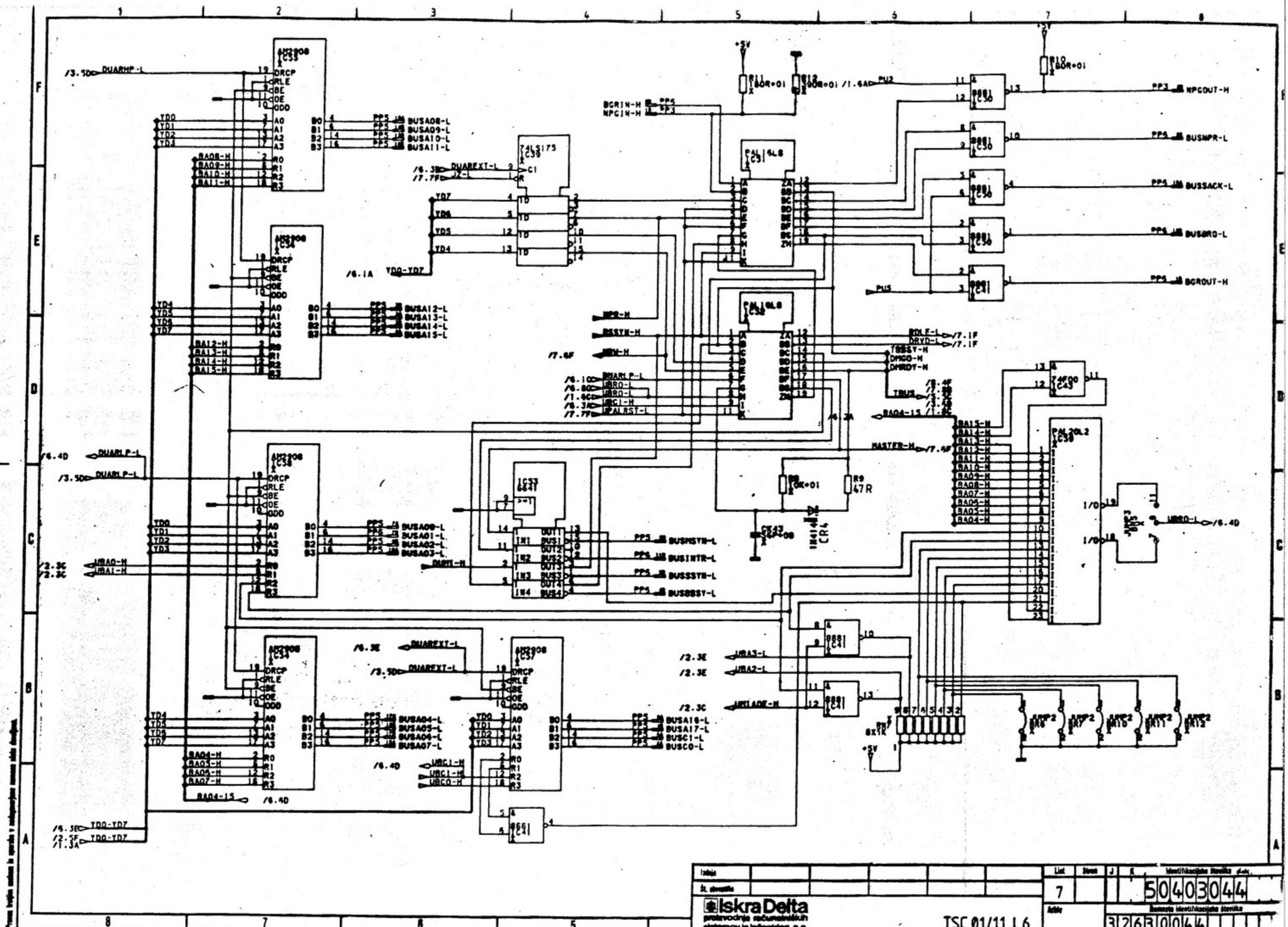
Obr. 42



tabja							List	Stran	J	K	Identifikacijska številka
Št. obvestila							5				50403044
Iskra Delta proizvodnja računalniških sistemov in inženiring, p.o.				TSC01/11 L4			Arhiv				32630044

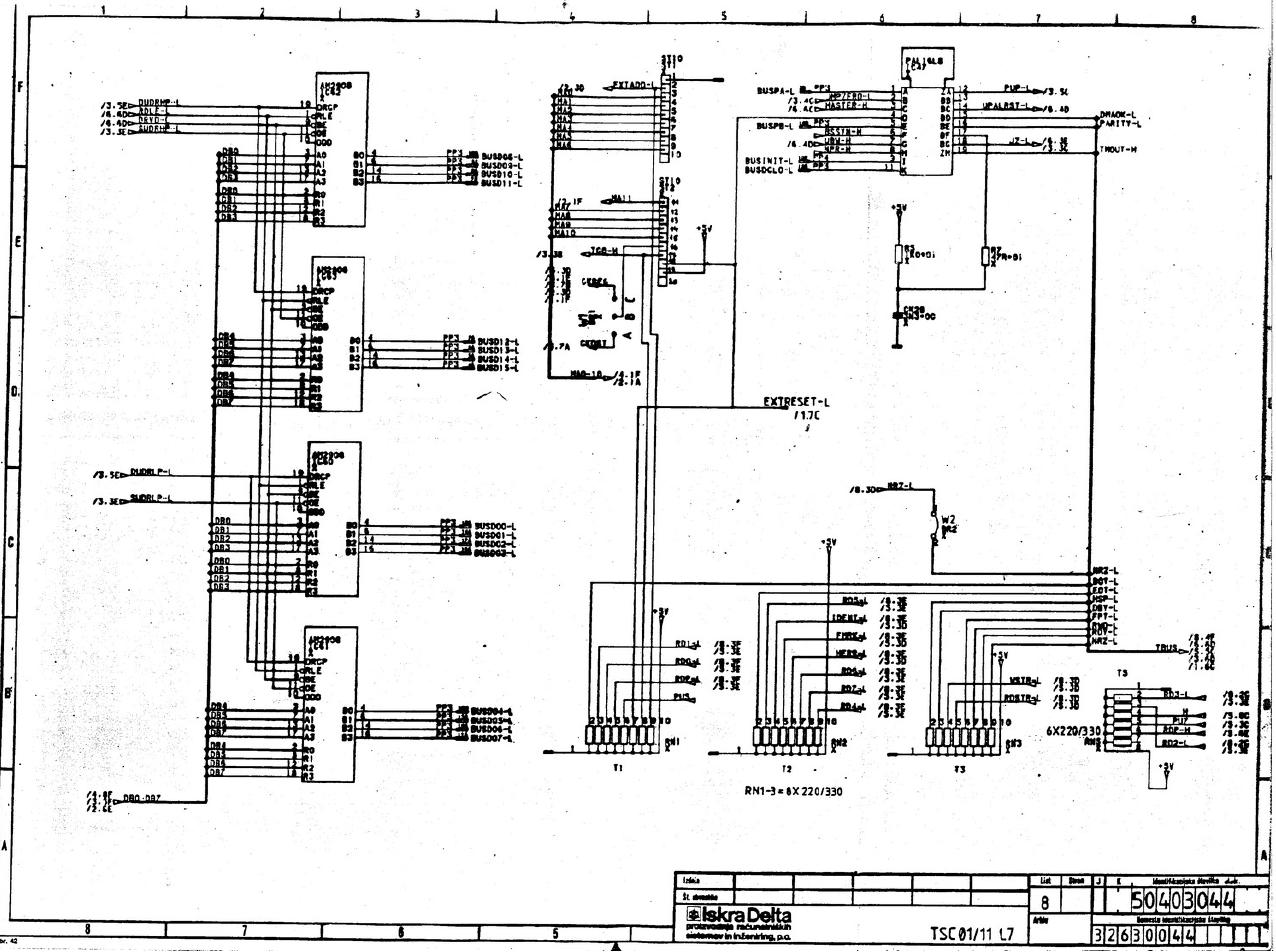


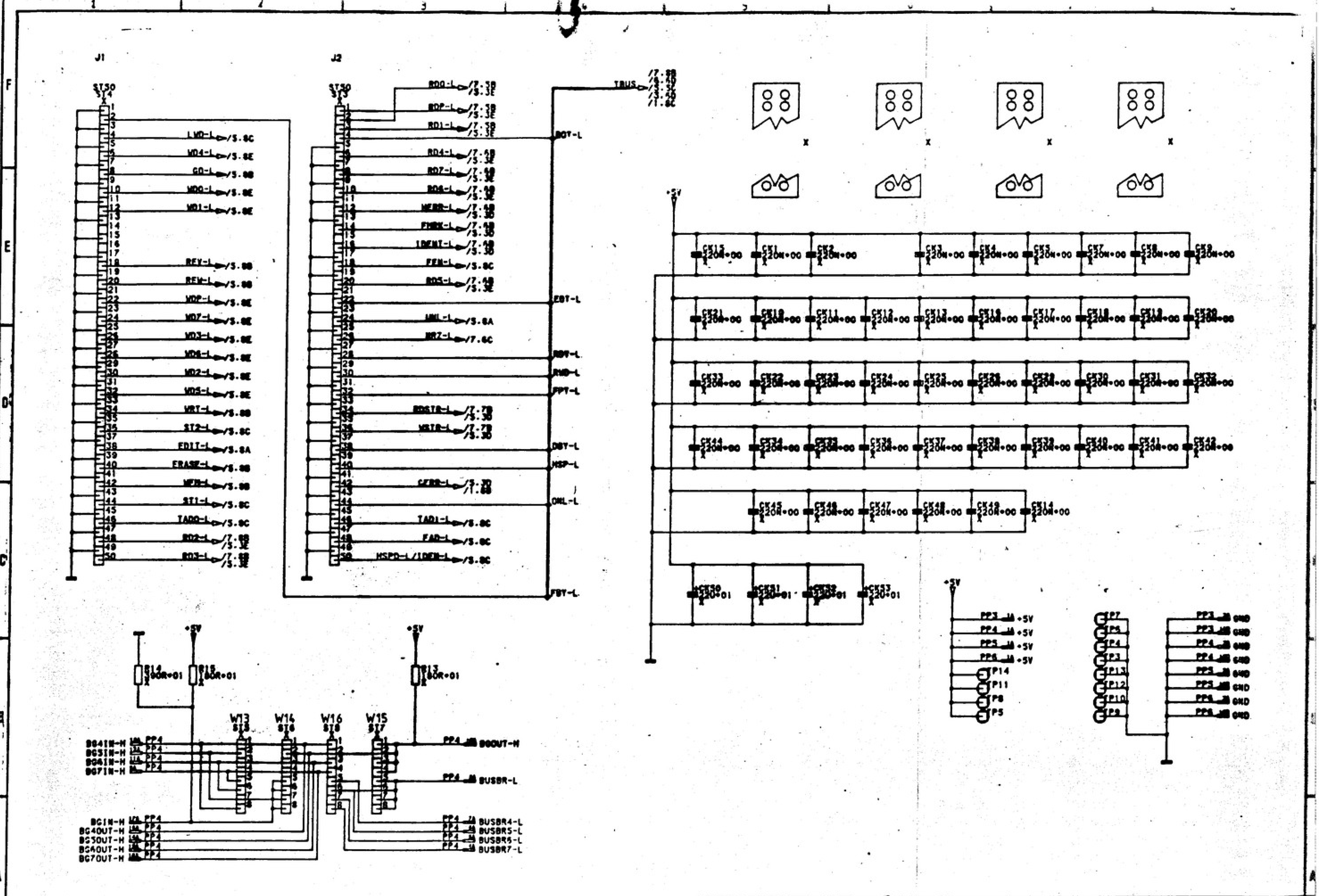
Izdaja						List	Stran	J	K	Identifikacijska številka dok.
Št. obvestila						6				50403044
Iskra Delta proizvodnja računalniških sistemov in inženiring, p.o.					TSC 01/11 LS	Arhiv	Namesto identifikacijske številke			32630044



Izdaja								List	Strani
Št. sprememb								7	
Iskra Delta proizvodnja računalniških sistemov in inženiring, p.o.								Arhiv	
TSC 01/11 L6								Identifikacijska številka plošče	
								50403044	
								Domača identifikacijska številka	
								32630044	

Obr. 42


AM2908 IC62
AM2908 IC63
AM2908 IC60
AM2908 IC61
DUDRHP-L
RDLE-L
DRYD-L
SUDRHP-L
DUDRLP-L
SUDRLP-L
BUSD08-L
BUSD09-L
BUSD10-L
BUSD11-L
BUSD12-L
BUSD13-L
BUSD14-L
BUSD15-L
BUSD00-L
BUSD01-L
BUSD02-L
BUSD03-L
BUSD04-L
BUSD05-L
BUSD06-L
BUSD07-L
DB0-DB7
EXTADD-L
MA11
TGO-H
MA0-10
EXTRESET-L
/1.7C
PAL16L8 IC47
BUSPA-L
HP/ZERO-L
MASTER-H
BUSPB-L
BSSYN-H
UBW-H
NPR-H
BUSINIT-L
BUSDCLO-L
PUP-L
UPALRST-L
JZ-L
DMAOK-L
PARITY-L
TMOUT-H
NRZ-L
W2
BOT-L
EOT-L
HSP-L
DBY-L
FPT-L
RWD-L
RDY-L
TBUS
RD1-L
RDG-L
RDP-L
PUS
RD5-L
IDENT-L
FMRK-L
HERR-L
RD6-L
RD7-L
RD4-L
WSTR-L
RDSTR-L
RD3-L
PUZ
RDP-H
RD2-L
RN1
RN2
RN3
RN5
T1
T2
T3
T5
6X220/330
RN1-3 = 8X 220/330
+5V
Iskra Delta
proizvodnja računalniških sistemov in inženiring, p.o.
TSC01/11 L7
List 8
50403044
32630044



Iskra Delta
proizvodnja računalniških sistemov in inženiring, p.o.

TSC 01/11 L8

List 9

Identifikacijska številka 5040304 4

Namesto identifikacijske številke 32630044